UNITED TECHNOLOGIES MOSTEK

MEMORY PRODUCTS DIVISION

1982/83 MEMORY DESIGNERS GUIDE

1982/1983
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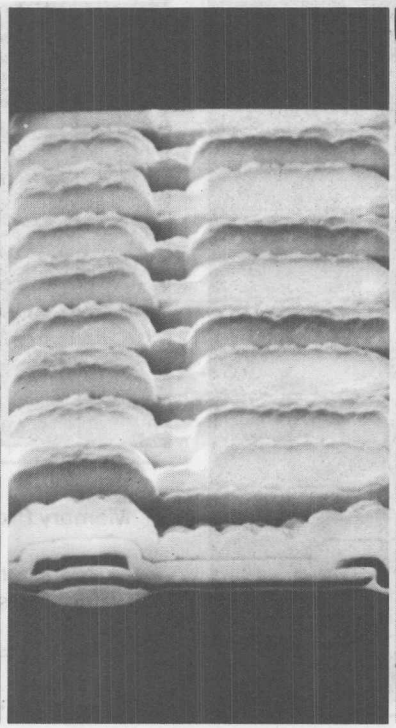
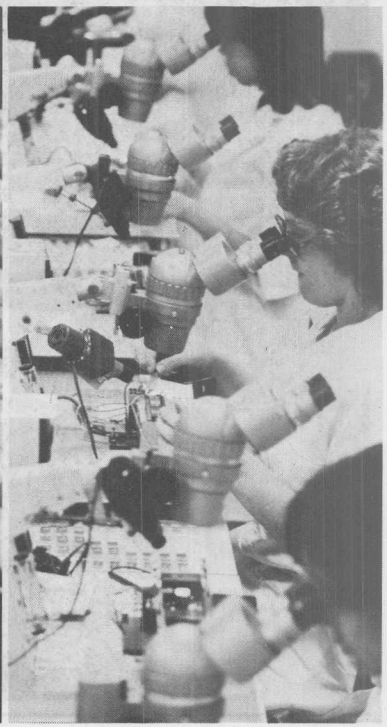




TECHNOLOGY

From its beginning, Mostek has been an innovator. From the developments of the 1K dynamic RAM and the single-chip calculator in 1970 to the current 64K dynamic RAM, Mostek technological breakthroughs have proved the benefits and cost-effectiveness of metal oxide semiconductors. Today, Mostek represents one of the industry's most productive bases of MOS/LSI technology, including Direct-Step-on-Wafer processing and laser implemented redundant circuitry.

The addition of the Microelectronics Research Center in Colorado Springs adds a new dimension to Mostek circuit design capabilities. Using the latest computer-aided design techniques, center engineers will be keeping ahead of the future with new technologies and processes.

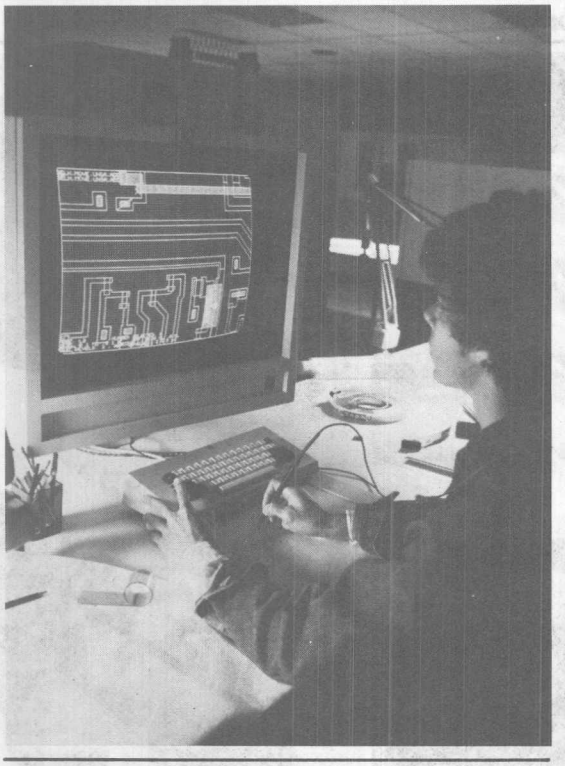
QUALITY

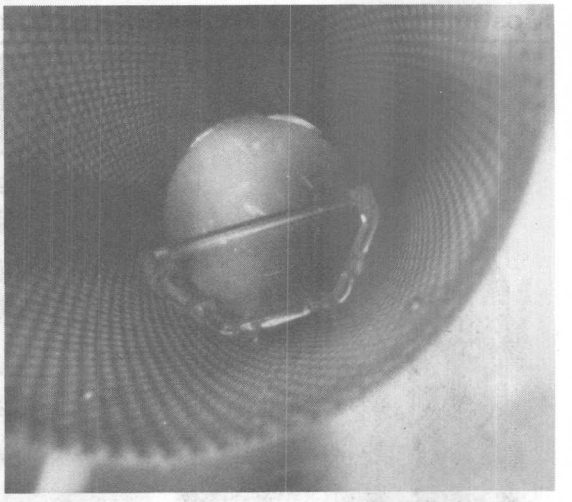
The worth of a product is measured by how well it is designed, manufactured and tested and by how well it works in your system.

In design, production and testing, the Mostek goal is meeting specifications the first time on every product. This goal requires a collective discipline from the company as well as individual efforts. Discipline, coupled with very personal pride, has enabled Mostek to build in quality at every level of production.

PRODUCTION CAPABILITY

The commitment to increasing production capability has made Mostek the world's largest manufacturer of dynamic RAMs. We entered the telecommunications market in 1974 with a tone dialer, and have shipped millions of telecom circuits since then. Millions of our MK3870 single-chip microcomputers are in use throughout the world. Recent construction in Dallas, Ireland and Colorado Springs has added some 50 percent to the Mostek manufacturing capacity.





THE PRODUCTS

Telecommunications Products

Mostek is the leading supplier of tone dialers, pulse dialers, and CODEC devices. As each new generation of telecommunications systems emerges, Mostek is ready with new generation components, including PCM filters, tone decoders, repertory dialers, new integrated tone dialers, and pulse dialers.

These products, many of them using CMOS technology, represent the most modern advancements in telecommunications component design.

Industrial Products

Mostek's line of Industrial Products offers a high degree of versatility per device. This family of components includes various microprocessor-compatible A/D converters, a counter/time-base circuit for the division of clock signals, and combined counter/display decoders. As a result of the low parts count involved, an economical alternative to discrete logic systems is provided.

Memory Products

Through innovations in both circuit design, wafer processing and production, Mostek has become the industry's leading supplier of dynamic RAMs.

Examples of Mostek leadership are families of x1 and x8 high performance static RAMs and our extremely successful 64K ROMs with more codes processed than any other mask-ROM in the industry. Another performance and density milestone is our 256K ROM, the MK38000. In MOS Dynamic RAMs, Mostek led the way as the world's leading supplier of 16K devices.

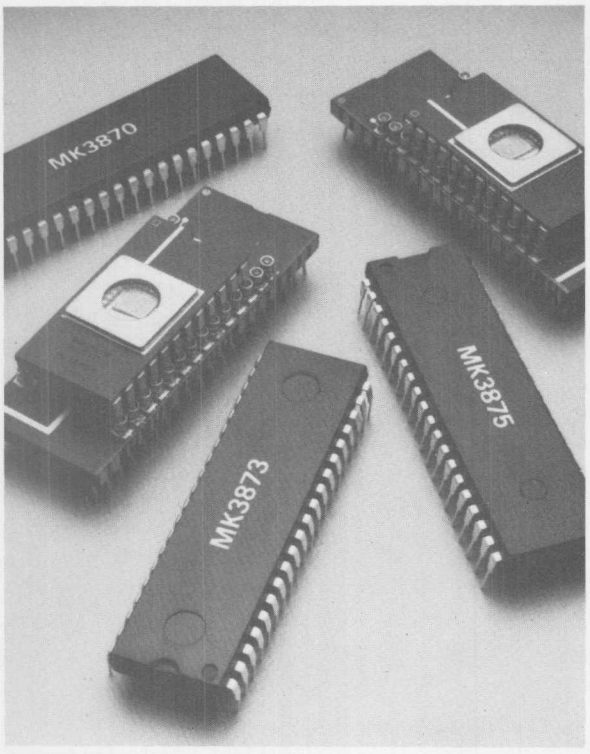
Our MK4564 64K dynamic RAM uses advanced circuit techniques and design to enhance manufacturability to satisfy the demands of a huge marketplace.

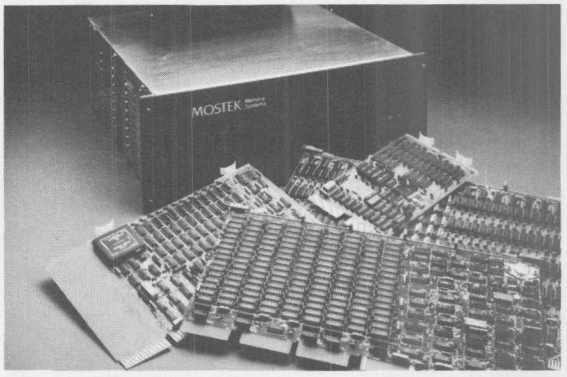
Microcomputer Components

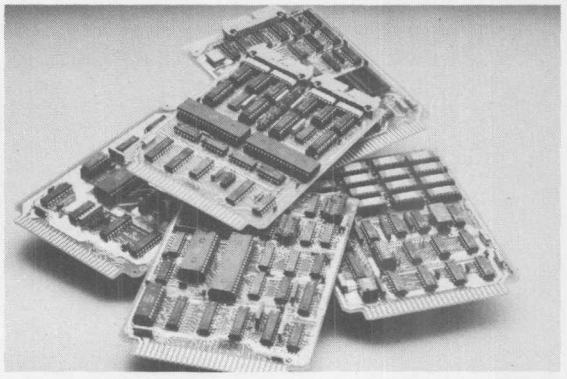
Mostek's microcomputer components cover the entire spectrum of microcomputer applications.

Our MK68000 16-bit microprocessor is designed for high-performance, memory-intensive systems.

Our Z80 is today's industry-standard 8-bit microprocessor. The Mostek 3870 family of single-chip microcomputers offers upgrade options in ROM, RAM, and I/O—all in the same socket. The MK38P70 EPROM piggyback microcomputer emulates the entire family and is ideal for low-volume applications.







Development systems include the RADIUS™ remote development station that lets you use your host minicomputer to develop the applications software. The program is then downloaded into the RADIUS which then lets you perform real-time in-circuit emulation and debug. The Mostek Matrix™ Development System is a stand-alone hardware and software debug and integration system.

Microcomputer Systems

Mostek is the world's leading manufacturer of Z80-based STD BUS system components. A new line of microsystems utilizing the VME BUS and based on the MK68000 will be available soon.

Computer systems include our Matrix line which utilize STD BUS cards to let you custom-design your own system.

Military Products

An extension of the high quality in fabrication and design inherent in Mostek's product line allows many of our ICs to be made available screened to MIL-STD-883. In addition, select parts are qualified to the rigors of MIL-M-38510 and are processed on our QPL certified lines.

The MKB product line begins with the complete Memory Products offering, and extends into microprocessors and gate arrays. Leadless Chip Carrier packaging and prepared customer SCDs address the particular needs of the military community.

Memory Systems

Taking full advantage of our leadership in memory components technology, Mostek Memory Systems offers a broad line of products, all with the performance and reliability to match our industry-standard circuits. Mostek Memory Systems offers add-in memory boards for popular DEC, Data General, and Perkin-Elmer minicomputers.

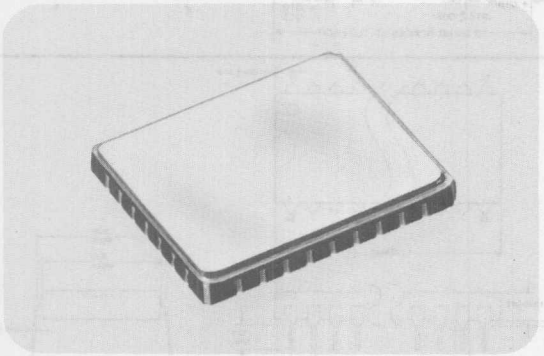
Mostek also offers special purpose and custom memory boards for special applications.

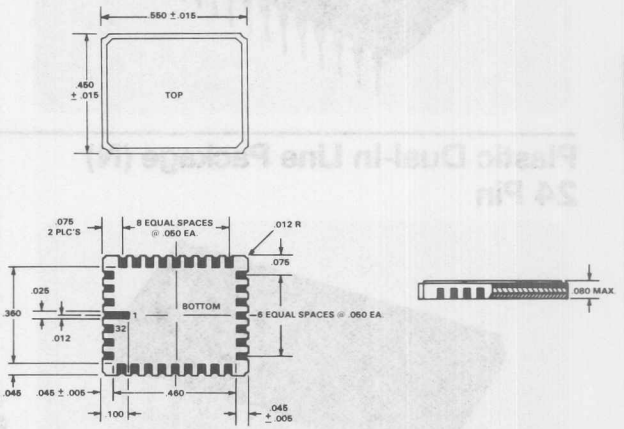
Gate Arrays

Utilizing the technology developed by United Technologies Microelectronic Research Center, Mostek plans to market custom gate array circuits in the second half of 1982.

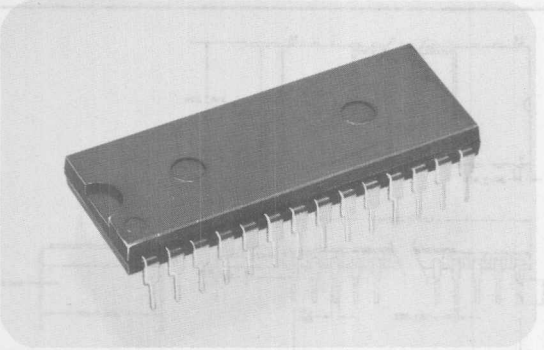
Package Descriptions

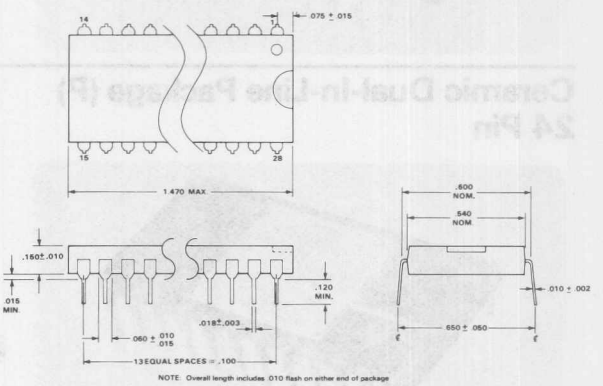
Leadless Hermetic Chip Carrier (E)
32 Pin (Proposed JEDEC Type E)



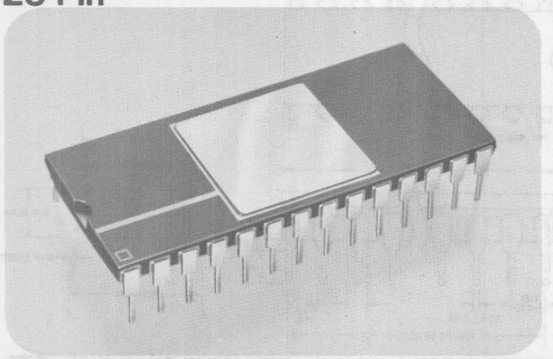


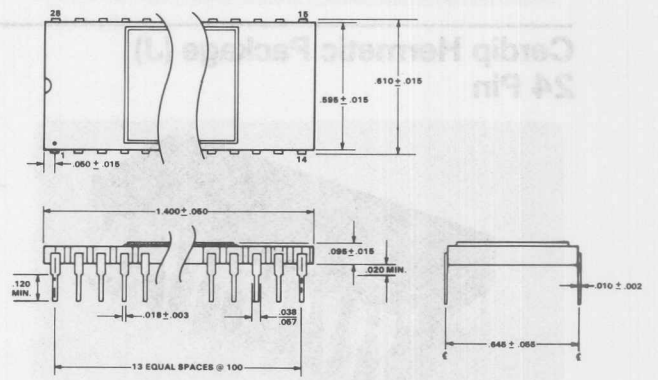
Plastic Dual-In-Line Package (N)
28 Pin



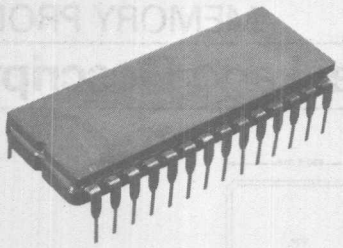


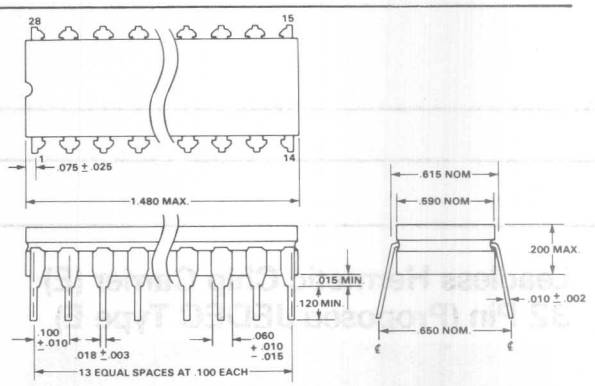
Ceramic Dual-In-Line Package (P)
28 Pin



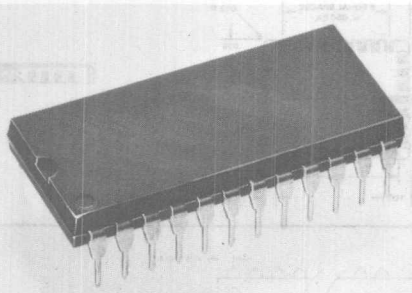


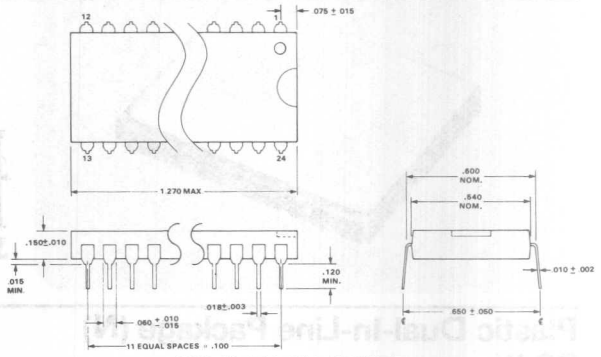
Cerdip Hermetic Package (J)
28 Pin





Plastic Dual-In Line Package (N)
24 Pin





Ceramic Dual-In-Line Package (P)
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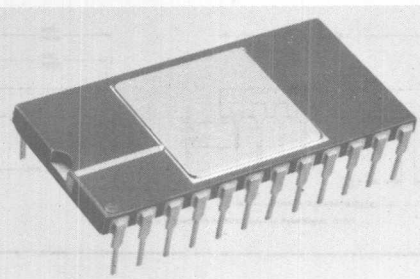
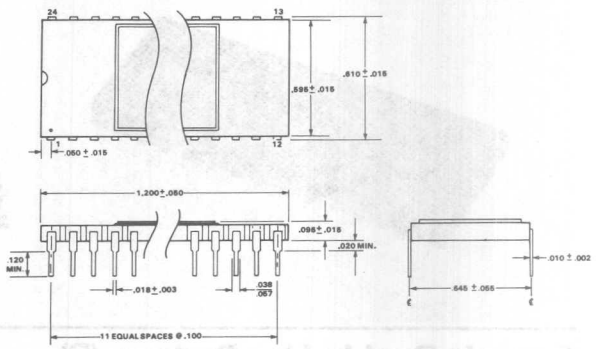
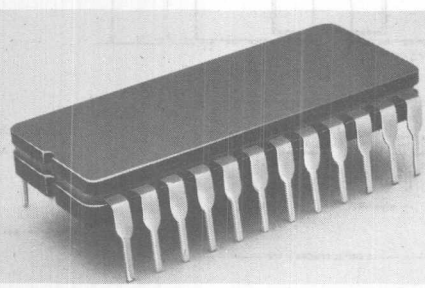
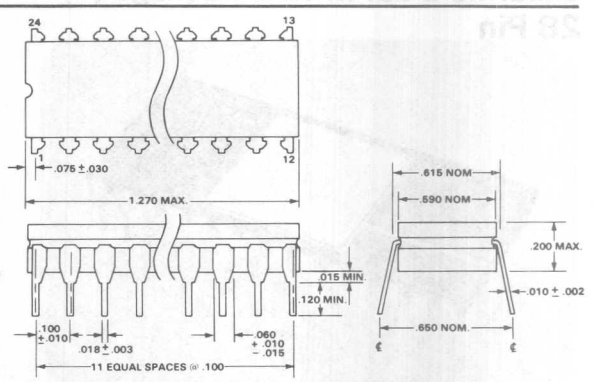


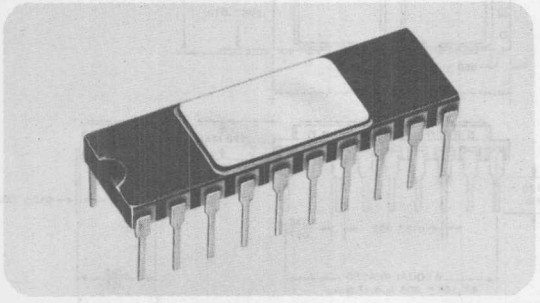


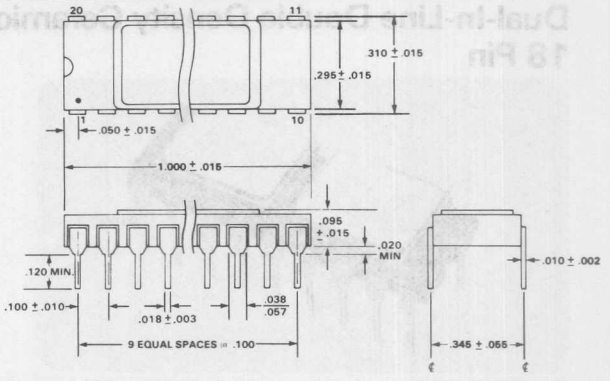
Cerdip Hermetic Package (J)
24 Pin





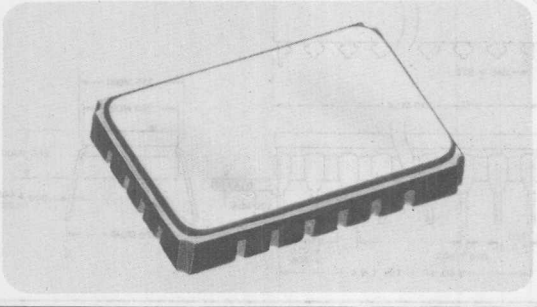
Ceramic Dual-In-Line Package (P)
20 Pin

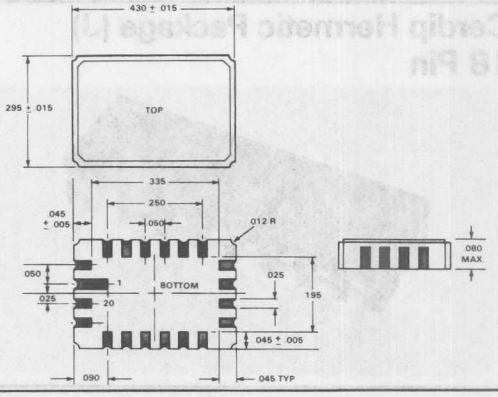




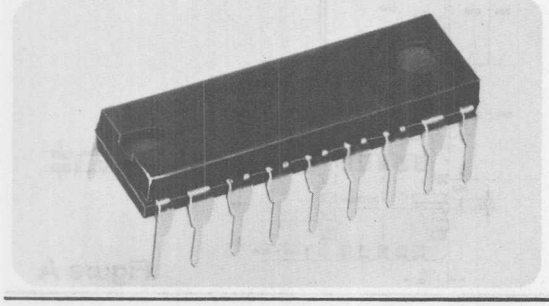
II

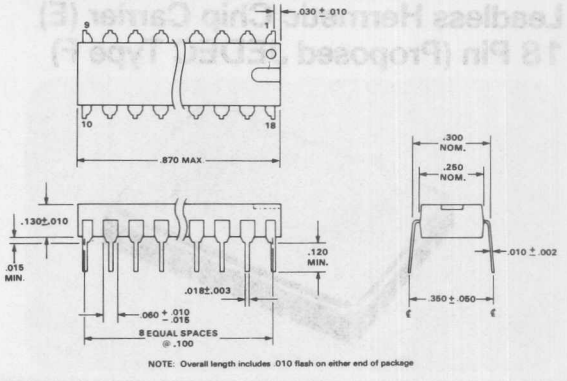
Leadless Hermetic Chip Carrier (E)
20 Pin





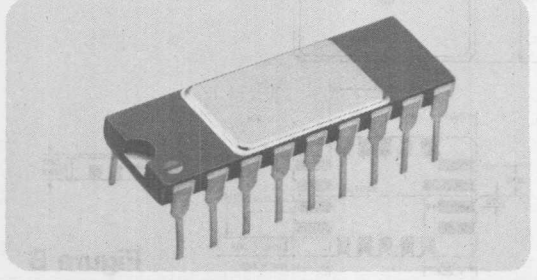
Plastic Dual-In-Line Package (N)
18 Pin

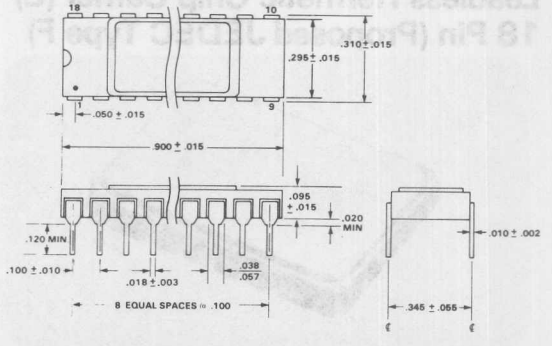




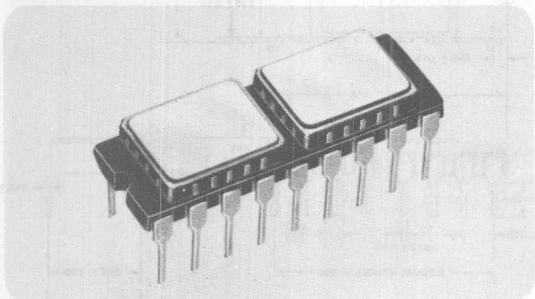
NOTE: Overall length includes .010 flash on either end of package

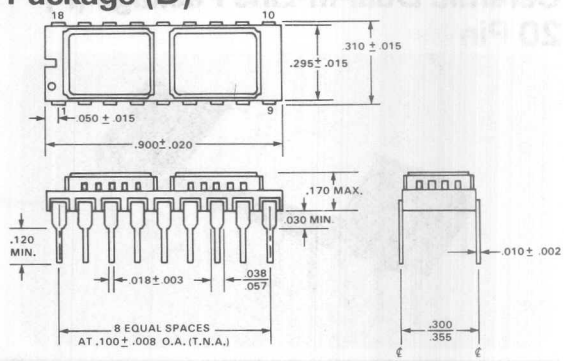
Ceramic Dual-In-Line Package (P)
18 Pin



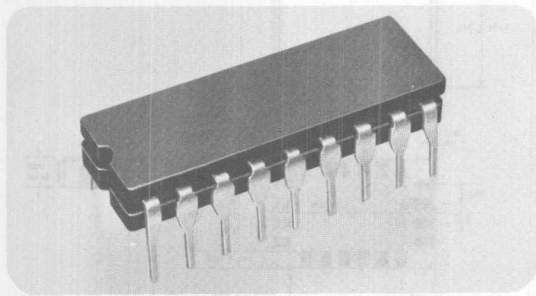


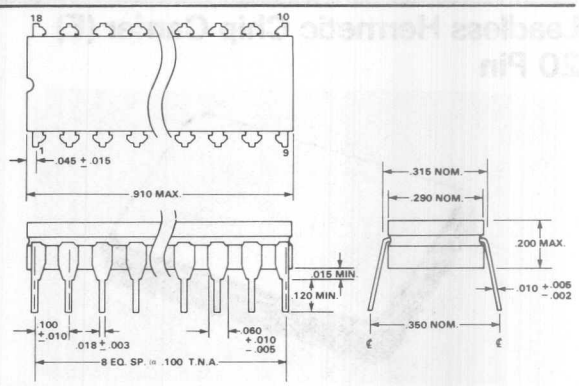
Dual-In-Line Double Density Ceramic Package (D)
18 Pin



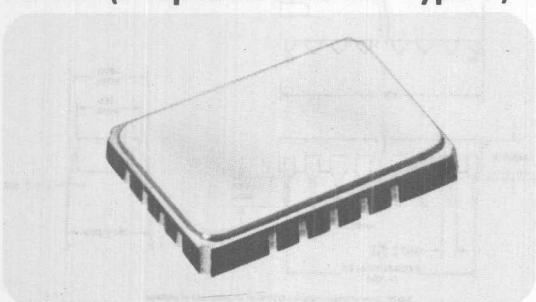


Cerdip Hermetic Package (J)
18 Pin





Leadless Hermetic Chip Carrier (E)
18 Pin (Proposed JEDEC Type F)



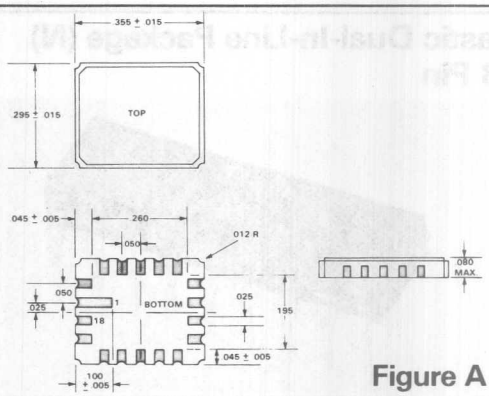


Figure A

Leadless Hermetic Chip Carrier (E)
18 Pin (Proposed JEDEC Type F)

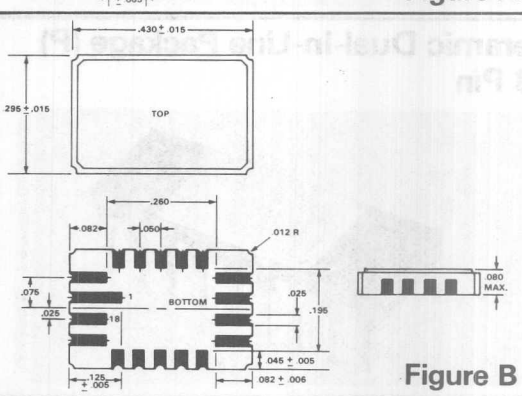
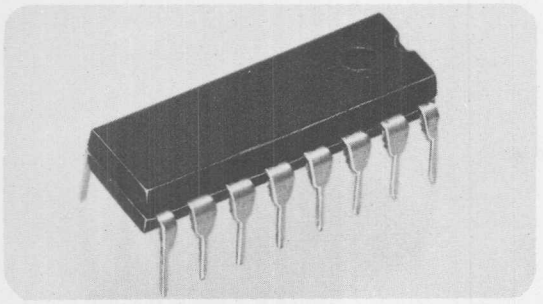
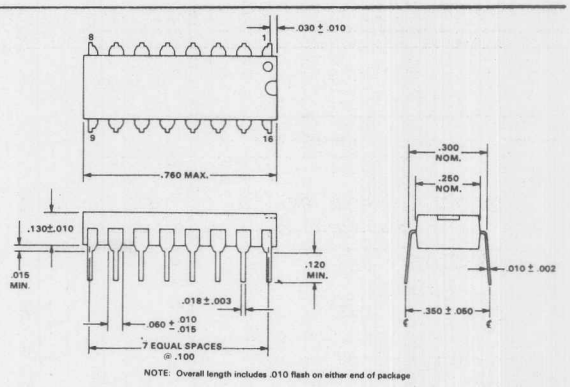


Figure B

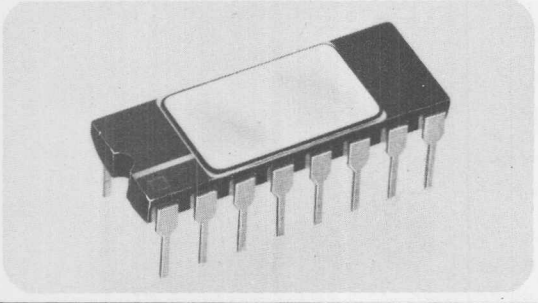
Plastic Dual-In-Line Package (N)
16 Pin

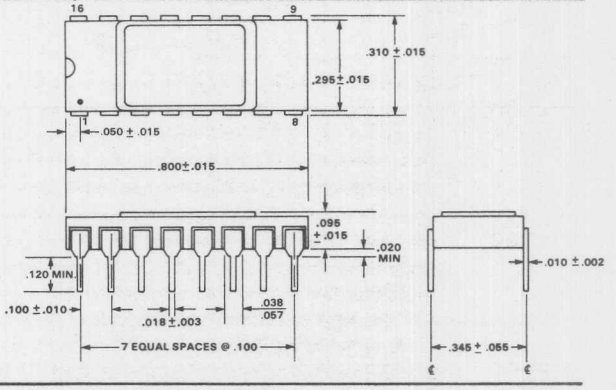




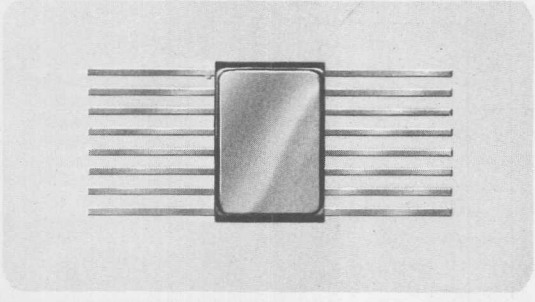
II

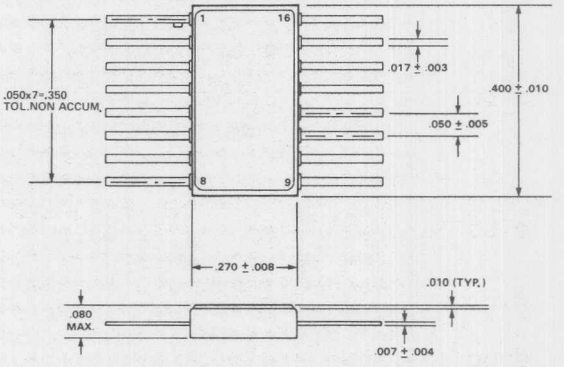
Ceramic Dual-In-Line Package (P)
16 Pin



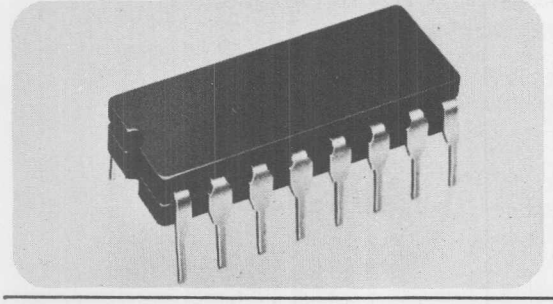


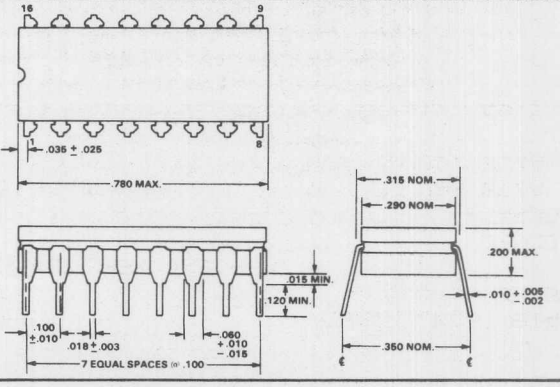
Ceramic Flat Package (F)
16 Pin

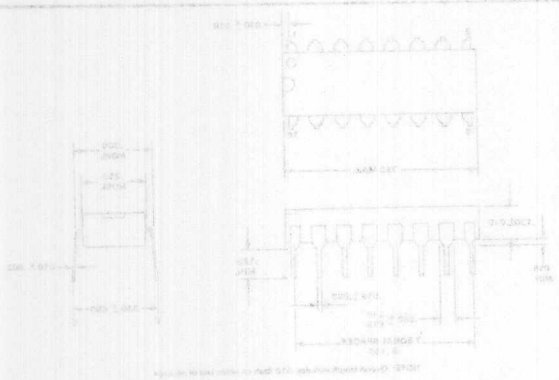


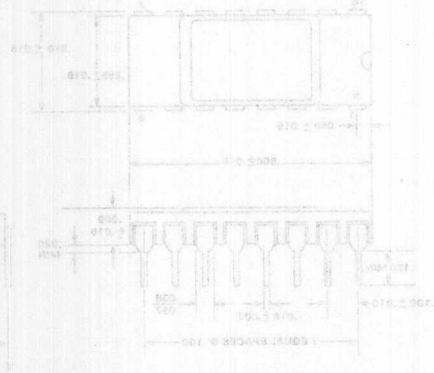


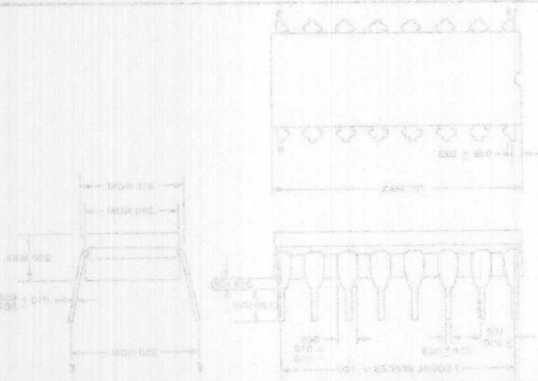
Cerdip Hermetic Package (J)
16 Pin



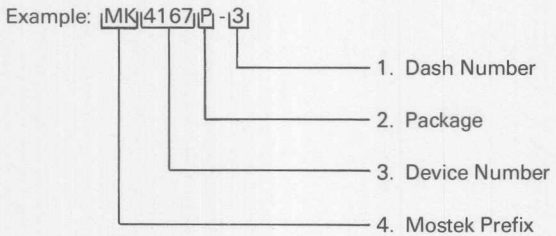








Factory orders for parts described in this book should include a four-part number as explained below:



1. Dash Number

   One or two numerical characters defining specific device performance characteristics and operating temperature range.

2. Package

   P - Gold side-brazed ceramic DIP
   N - Epoxy DIP (Plastic)
   K - Tin side-brazed ceramic DIP
   T - Ceramic DIP with transparent lid
   E - Ceramic leadless chip carrier
   D - Dual density RAM-PAC
   F - Flat pack

3. Device number

   1XXX or 1XXXX - Shift Register, ROM
   2XXX or 2XXXX - ROM, EPROM
   3XXX or 3XXXX - ROM, EPROM
   38XX - Microcomputer Components
   4XXX or 4XXXX - RAM
   5XXX or 5XXXX - Counters, Telecommunication and Industrial
   7XXX or 7XXXX - Microcomputer Systems

4. Mostek Prefix

   MK - Standard Prefix

1982/1983 MEMORY DESIGNERS GUIDE

TERMINAL CHARACTERISTICS OF THE 64K RAM

Application Note

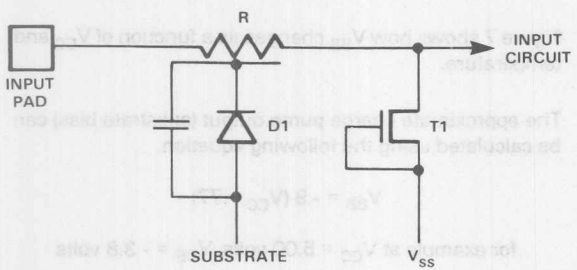
INTRODUCTION

This application note describes the input characteristics of the 64K RAM*. Each input pin has different requirements, depending upon its function as an address, clock, data-in or data-out.

1. INPUT PROTECTION CIRCUIT

All pins (excluding V_{CC}, V_{SS} and Data Out) have the input protection circuit shown in Figure 1 integrated onto the chip. The purpose of the circuit is to protect the 64K RAM from damage caused by the large voltages generated from static electricity. Static electricity may be encountered during all stages of the manufacturing process, during shipping and during handling by the customer.

INPUT PROTECTION CIRCUIT
Figure 1

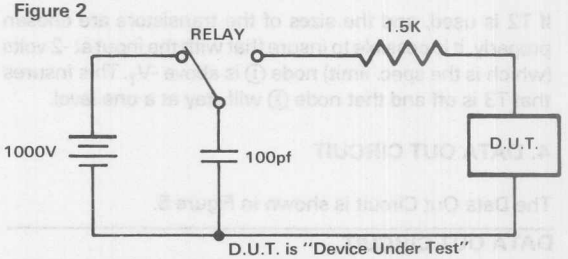


T1 is a transistor with BVDS (breakdown voltage drain to source) approximately equal to +18 volts. R and D1 are formed by an n^+ implanted resistor and the associated n^+/p^- diode. This resistance along with the parasitic capacitance act to attenuate fast rise time large positive voltage spikes. The non-destructive breakdown of T1 at 18 volts is less than the destructive oxide breakdown of transistors in the input circuit.

The input protection circuit is tested by the circuit shown in Figure 2. A 100pf capacitor is charged up to 1000 volts, then discharged through a 1.5KΩ resistor.

The supply pin V_{CC} (Pin 8), the ground pin V_{SS} (Pin 16) and the Data Out pin (Pin 14) do not have input protection circuits but rather rely on the large n^+ implanted regions to sink the static electricity generated current. Experience has shown these to be the best protected pins.

STATIC INPUT PROTECTION TEST CIRCUIT
Figure 2

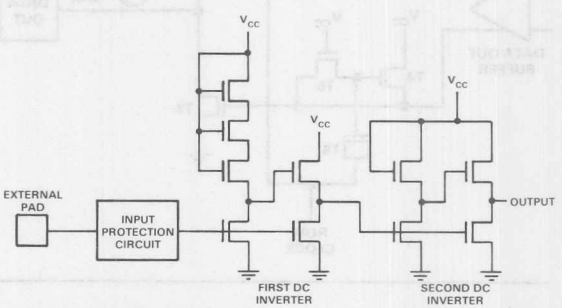


2. CLOCK INPUT CIRCUITS ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{RFSH}$)

The circuit used for the clock inputs is shown in Figure 3.

The purpose of this circuit is to insure TTL voltage level compatability. By proper device sizing the mid point of the transfer characteristics can be set to about 1.4V and vary little with threshold changes. Schmoo plots that show how V_{IL} and V_{IH} vary with V_{CC} are included.

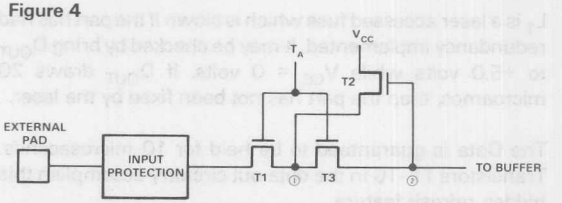
CLOCK INPUT CIRCUIT
Figure 3



3. ADDRESS AND DATA-IN, INPUT CIRCUITS

The circuitry used for address and data is shown in Figure 4.

ADDRESS/DATA INPUT CIRCUITS (TRAP PORTION)
Figure 4



T1 and T3 comprise the trap portion of the input circuit. When T_A (trap clock) goes low, whatever voltage is on nodes ① and ② is trapped there, even if the input voltage changes. Transistor T2 helps guard against a negative voltage on the column address.

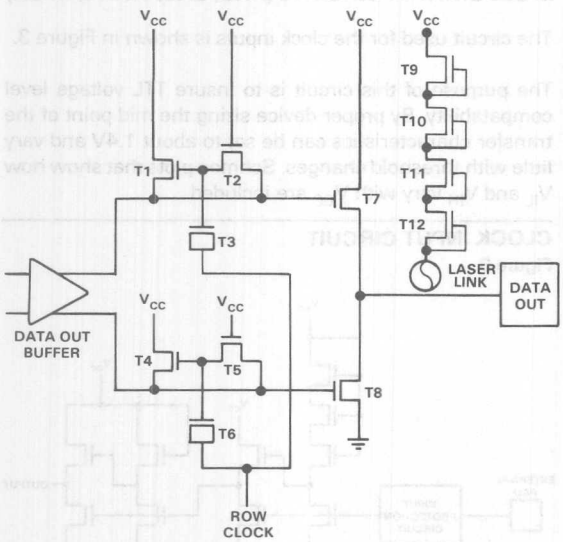
If the row address is a one level followed by the column address which is a zero level and the zero level is a negative voltage, it is possible that the one level stored on nodes ① and ② could be lost. If T_A is at ground and the external input is more than a $-V_T$ (about -.5V) then T1 will be on and node ① will be discharged.

If T2 is used, and the sizes of the transistors are chosen properly, it is possible to insure that with the input at -2 volts (which is the spec. limit) node ① is above $-V_T$. This insures that T3 is off and that node ② will stay at a one level.

4. DATA OUT CIRCUIT

The Data Out Circuit is shown in Figure 5.

DATA OUT CIRCUIT
Figure 5



A standard inverter is used. T_7 and T_8 are physically quite large to insure TTL compatability. V_{OH} = 2.4V @ 5ma source current. V_{OL} = .4V @ 4.2ma sink current. Schmoo plots are included which show the performance of this circuit.

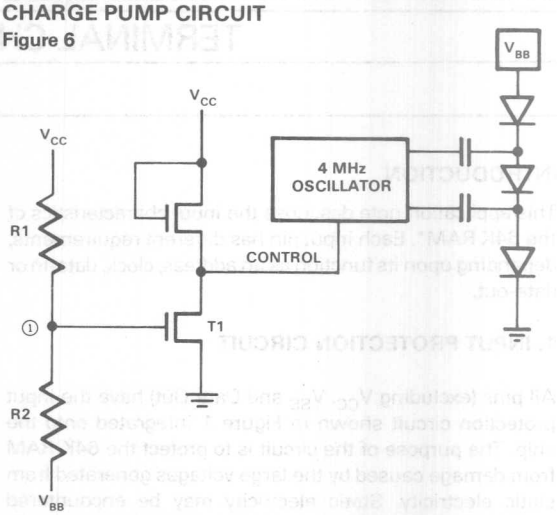
L_1 is a laser accessed fuse which is blown if the part has had redundancy implemented. It may be checked by bring D_{OUT} to +5.0 volts while V_{CC} = 0 volts. If D_{OUT} draws 20 microamps, then the part has not been fixed by the laser.

The Data is guaranteed to be held for 10 microseconds. Transistors T1 -T6 in the data out circuitry accomplish this hidden refresh feature.

5. SUBSTRATE BIAS GENERATOR

A charge pump circuit is used to generate the negative substrate bias required for proper circuit operation. The basic circuit used is shown in Figure 6.

CHARGE PUMP CIRCUIT
Figure 6



R1 and R2 form a resistor divider between V_{CC} and V_{BB}. If V_{BB} is very negative, the voltage on node ① is less than the threshold voltage of T1. The control signal is a high voltage and the charge pump is off.

Figure 7 shows how V_{BB} changes as a function of V_{CC} and temperature.

The approximate charge pump output (substrate bias) can be calculated using the following equation.

$$V_{BB} = -.9\,(V_{CC} - .77)$$

for example at V_{CC} = 5.00 volts, V_{BB} = - 3.8 volts

The charge pump output is a function of V_{CC} as previously stated. For increases in V_{CC}, the charge pump takes time to establish the correct substrate bias as shown in Figure 8.

The response of the charge pump to positive increases in V_{CC} is approximately:

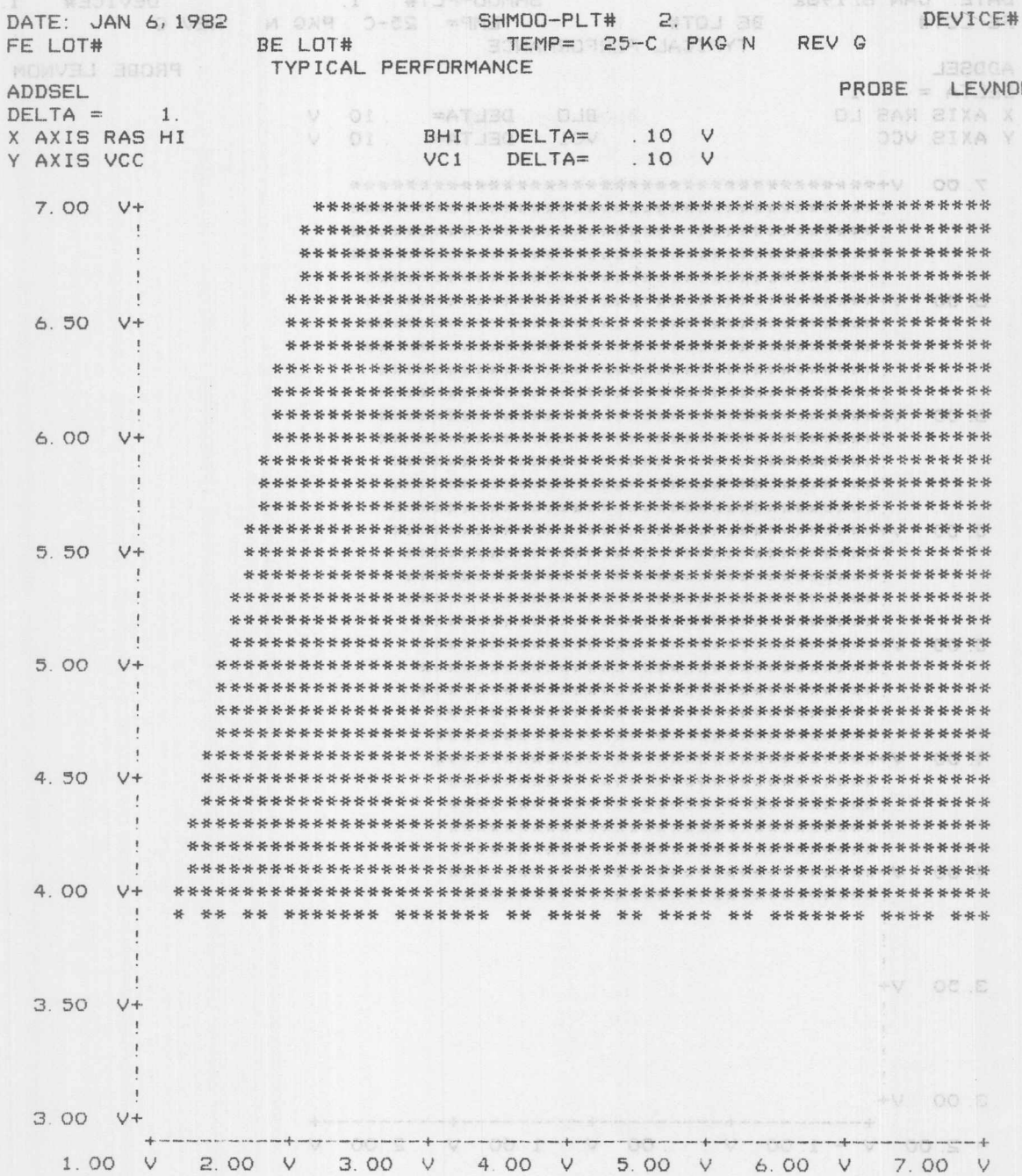
$$\frac{d\,V_{BB}}{d\,V_{CC}}$$

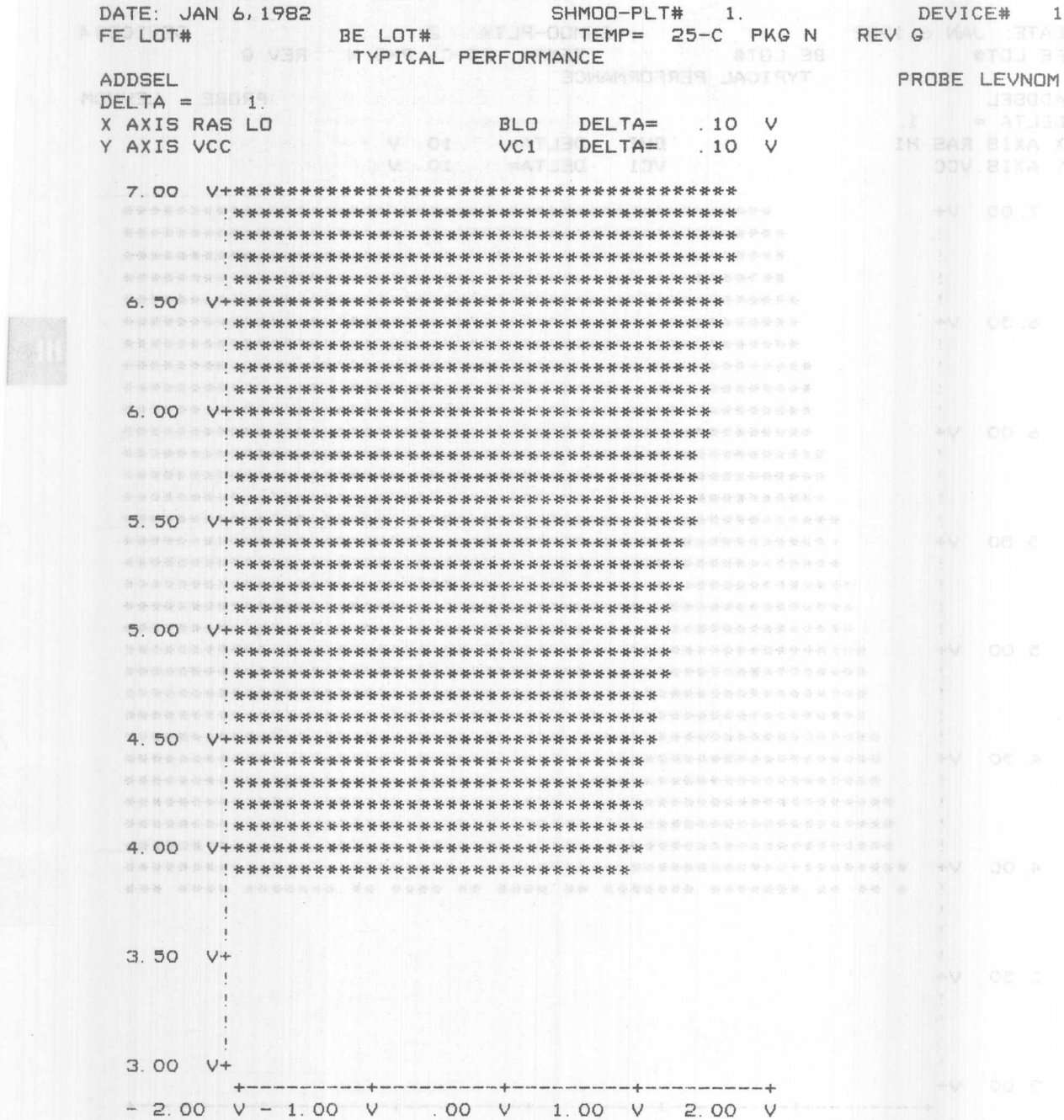
$$= .06 \text{ volts} / \mu\text{sec}$$

For example, when V_{CC} increases from 0 to 5 volts, V_{BB} changes from 0 to -3 volts. This requires about 48 μsec for V_{BB} to reach its final value.

Please note that we have assumed that the time required to change V_{CC} is negligibly small compared to the time for V_{BB} to change.

TYPICAL V_{IH} VERSUS V_{CC} FOR CLOCK INPUTS




DATE: JAN 6, 1982
SHMOO-PLT# 1.
DEVICE# 1.
FE LOT#
BE LOT#
TEMP= 25-C
PKG N
REV G
TYPICAL PERFORMANCE
ADDSEL
PROBE LEVNOM
DELTA = 1.
X AXIS RAS LO
BLO
DELTA= .10 V
Y AXIS VCC
VC1
DELTA= .10 V
7.00 V
6.50 V
6.00 V
5.50 V
5.00 V
4.50 V
4.00 V
3.50 V
3.00 V
- 2.00 V
- 1.00 V
.00 V
1.00 V
2.00 V

SHMOO-PLT# 1. DEVICE# 2.

FE LOT# BE LOT# TEMP= 25-C PKG N REV G

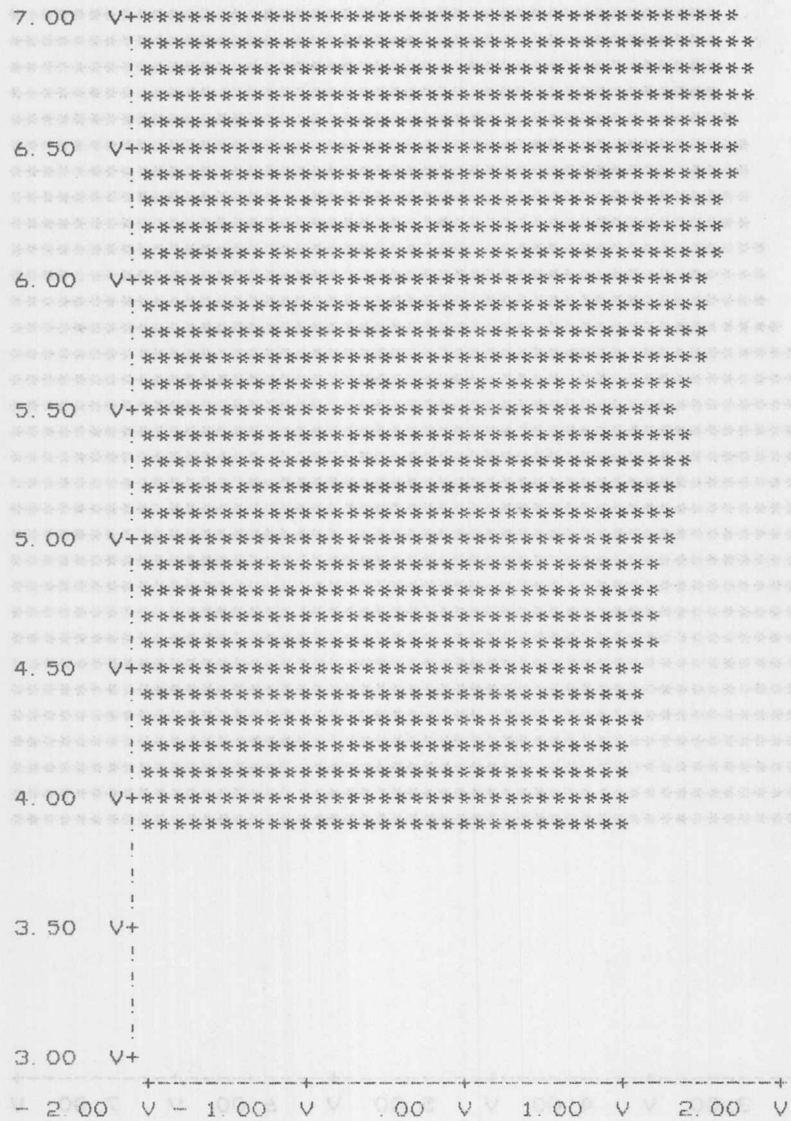
TYPICAL PERFORMANCE

ADDSEL PROBE LEVNOM

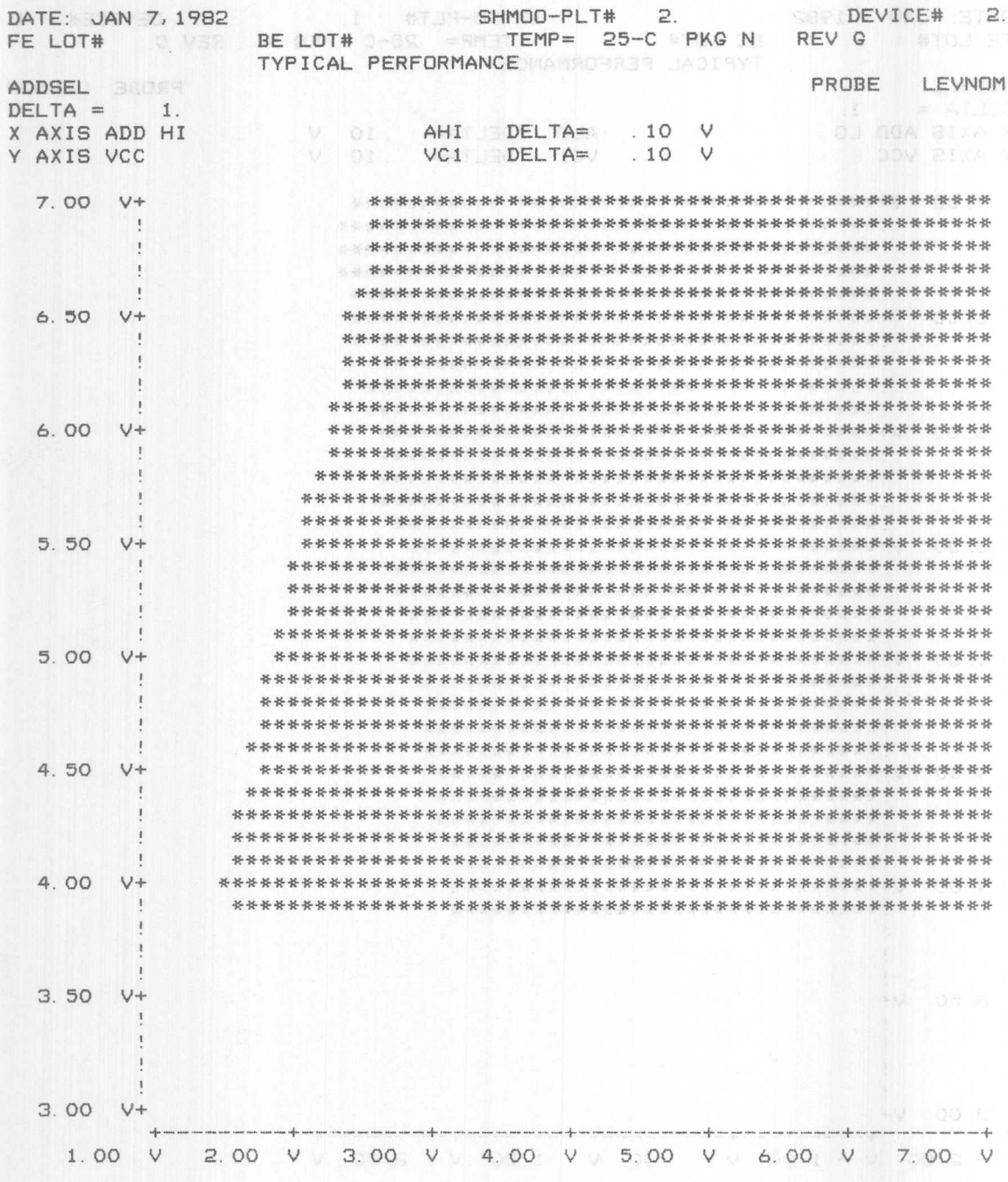
DELTA = 1.

X AXIS ADD LO ALO DELTA= .10 V

Y AXIS VCC VC1 DELTA= .10 V

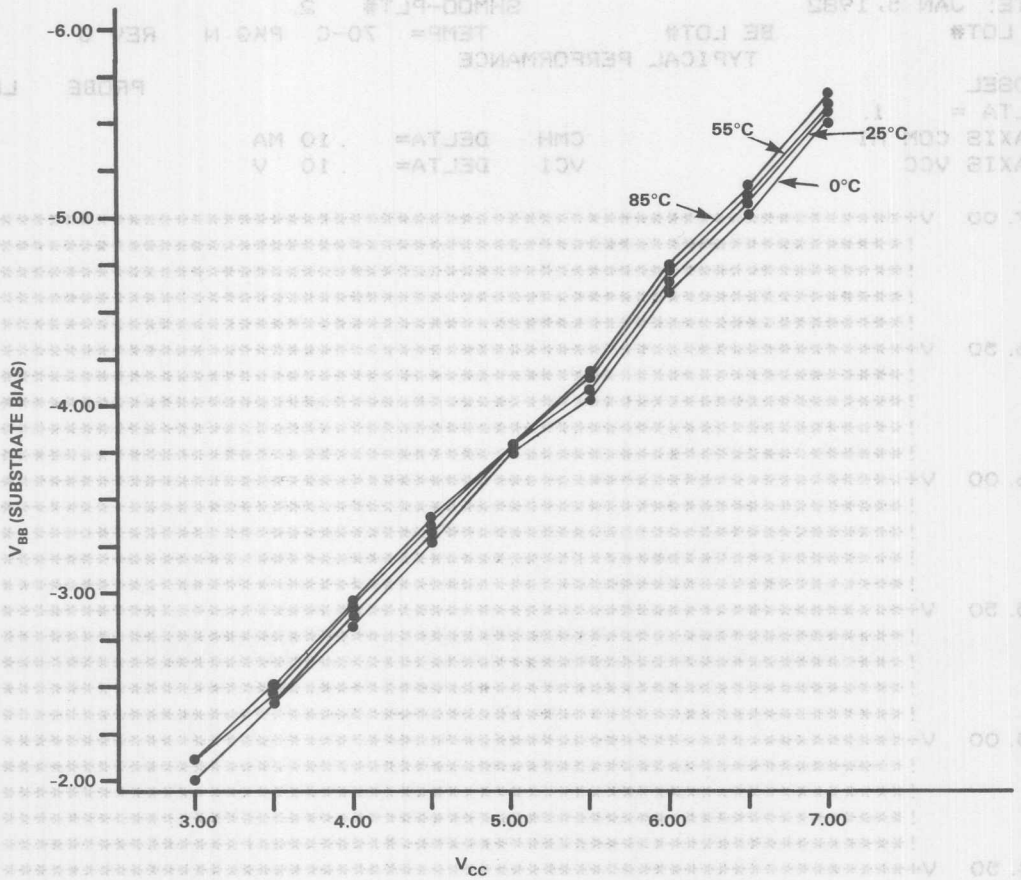


V_{IH} VERSUS V_{CC} FOR ADDRESS BUFFER



CHARGE PUMP OUTPUT vs V_{CC} vs TEMPERATURE

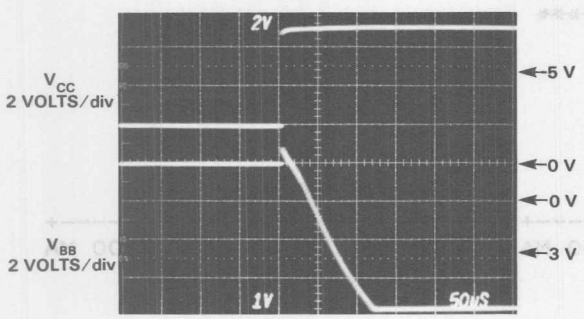
Figure 7



III

RESPONSE OF V_{BB} TO POSITIVE INCREASES IN V_{CC} AT ROOM TEMPERATURE

Figure 8



If V_{CC} decreases, the charge pump will be in its of state, and V_{BB} will gradually become more positive as the substrate leaks towards ground. Figure 9 shows the response of V_{BB} as V_{CC} decreases.

The change in V_{BB} would follow this equation.

$$V_{BB}(t) = V_{BB}\ (1) - e^{-t/\tau} \quad \text{for } V_{BB}\ (t) < V_{BB}\ (\text{final})$$

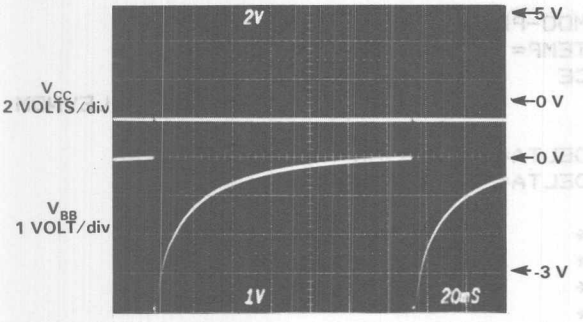
The substrate bias starts decaying at a rate as if it's going to ground. When V_{BB} (t) reaches a point where the charge pump turns on, the substrate bias stays at that constant value.

```
DATE: JAN 5, 1982                    SHMOO-PLT#    2.
FE LOT#          BE LOT#              TEMP=  70-C  PKG N   REV G
                  TYPICAL PERFORMANCE
ADDSEL                                                    PROBE   LEVNOM
DELTA =     1.
X AXIS COM HI                    CMH   DELTA=    .10 MA
Y AXIS VCC                       VC1   DELTA=    .10  V

  7.00  V+*************************************************************
        !*************************************************************
        !*************************************************************
        !*************************************************************
        !*************************************************************
  6.50  V+*************************************************************
        !*************************************************************
        !*************************************************************
        !*************************************************************
        !*************************************************************
  6.00  V+*************************************************************
        !*************************************************************
        !*************************************************************
        !*************************************************************
        !*************************************************************
  5.50  V+*************************************************************
        !*************************************************************
        !*************************************************************
        !*************************************************************
        !*************************************************************
  5.00  V+*************************************************************
        !*************************************************************
        !*************************************************************
        !*************************************************************
        !*************************************************************
  4.50  V+*************************************************************
        !*************************************************************
        !*************************************************************
        !*************************************************************
        !*************************************************************
  4.00  V+*************************************************
        !*************************************
        !*********************************
        !*****************************
        !*************************
  3.50  V+*********************
        !**************
        !****
        !
        !
  3.00  V+
        +---------+---------+---------+---------+---------+---------+
    1.00 MA   2.00 MA   3.00 MA   4.00 MA   5.00 MA   6.00 MA   7.00 MA
```

```
DATE: JAN 5, 1982                    SHMOO-PLT#    1.
FE LOT#          BE LOT#                TEMP=  70-C  PKG N   REV G
                   TYPICAL PERFORMANCE
ADDSEL                                                    PROBE   LEVNOM
DELTA =     1.
X AXIS COM LO                        CML    DELTA=-   .20 MA
Y AXIS VCC                           VC1    DELTA=    .10  V

  7.00  V+******************************
        !******************************
        !******************************
        !******************************
        !******************************
  6.50  V+******************************
        !******************************
        !******************************
        !******************************
        !******************************
  6.00  V+******************************
        !******************************
        !******************************
        !******************************
        !******************************
  5.50  V+******************************
        !******************************
        !******************************
        !******************************
        !******************************
  5.00  V+******************************
        !******************************
        !******************************
        !******************************
        !******************************
  4.50  V+******************************
        !****************************
        !****************************
        !****************************
        !****************************
  4.00  V+****************************
        !
        !
        !
        !
  3.50  V+
        !
        !
        !
        !
  3.00  V+
        +----------+----------+----------+----------+
    .00 MA - 2.00 MA - 4.00 MA - 6.00 MA - 8.00 MA
```

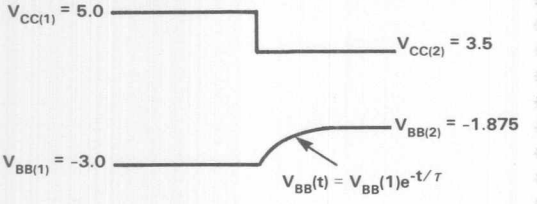
V_{BB} RESPONSE TO V_{CC} CHANGING FROM +5 V TO 0 V AT T=25°C

Figure 9



τ is measured to be approximately 22 ms.

As an example suppose $V_{CC}(1) = 5.0$ volts and $V_{CC}(2) = 3.5$ volts. Using $V_{BB} = -.75 (V_{CC} - 1)$ then $V_{BB}(1) = -3.0$ volts, and $V_{BB}(2) = -1.875$ volts.



To calculate the time required for V_{BB} to change from -3.0 volts to -1.875 volts, use the equation

$$V_{BB}(t) = V_{BB}(1)\, e^{-t/\tau}$$

Solve for t

$$e^{t/\tau} = \frac{V_{BB}(1)}{V_{BB}(t)}$$

$$t = \tau \ln \left[\frac{V_{BB}(1)}{V_{BB}(t)} \right]$$

Substitute:

$$t = 22 \text{ ms} \ln \left[\frac{-3.0}{-1.875} \right]$$

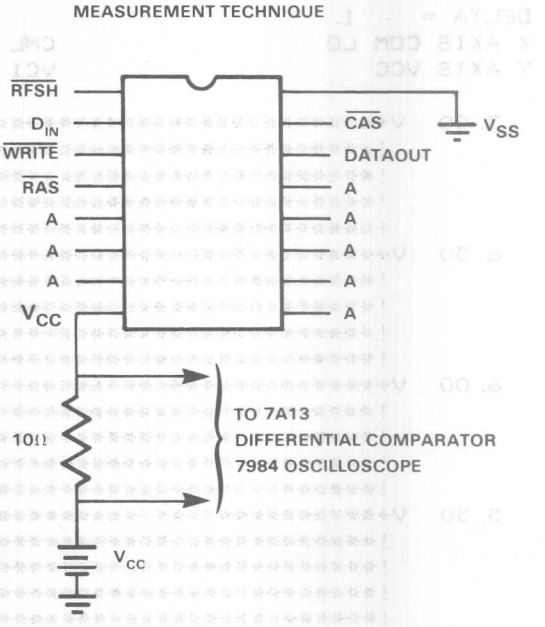
$t = 10.34$ ms

6. SUPPLY CURRENTS

I_{CC} is shown on a typical device for various types of cycles and conditions.

CIRCUIT FOR MEASUREMENT OF I_{CC}

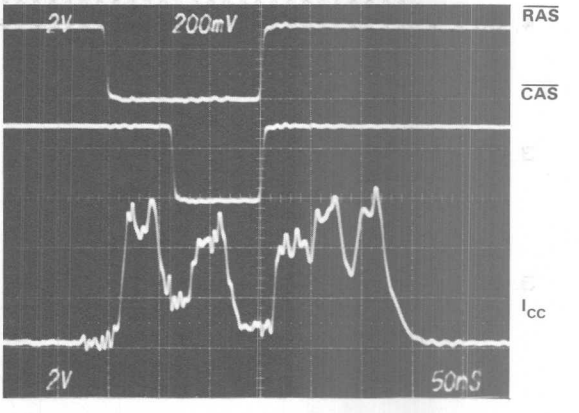
Figure 10



NOTE: All waveforms were measured at room temperature, $V_{CC} = 5.0$ volts.

WRITE CYCLE (EARLY WRITE)

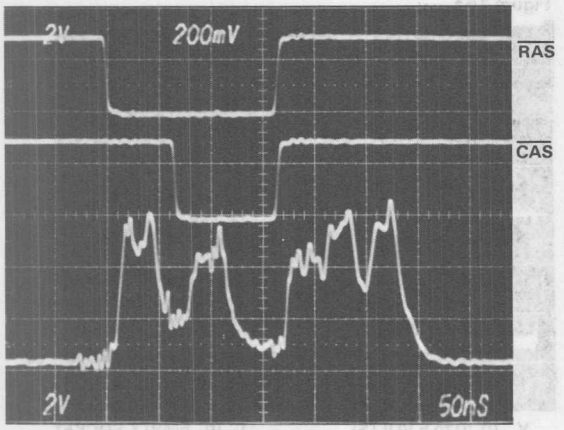
Figure 11



VERTICAL SCALE: 20 ma/div $t_{RC} = 1000$ns

I_{CC} DURING READ/WRITE CYCLE (LATE WRITE)

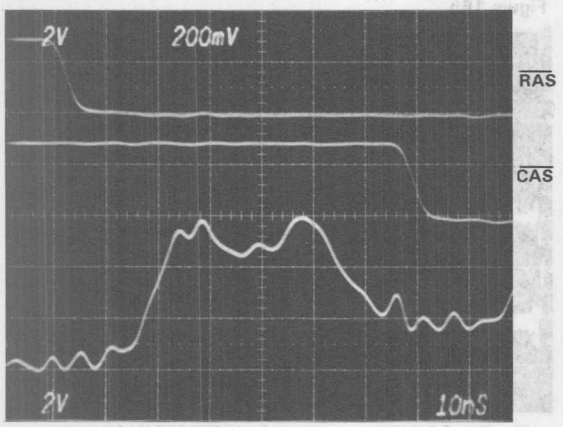
Figure 12a



VERTICAL SCALE: 20 ma/div

EXPANDED VIEW OF $I_{CC}(t)$ FOLLOWING $\overline{RAS}$

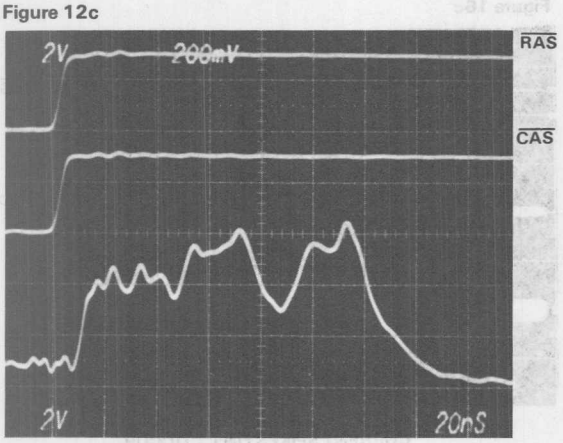
Figure 12b



VERTICAL SCALE: 20 ma/div

EXPANDED VIEW OF $I_{CC}(t)$ DURING $\overline{RAS}$ PRECHARGE

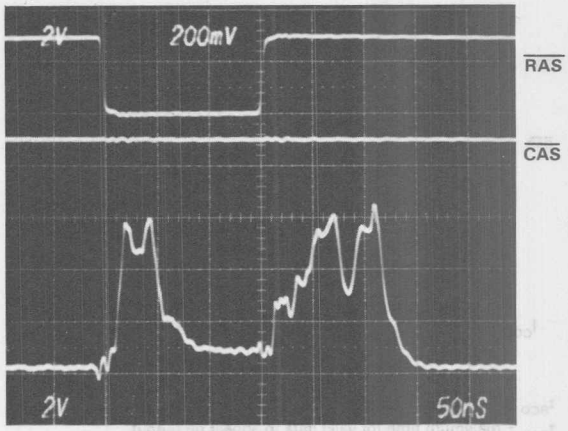
Figure 12c



VERTICAL SCALE: 20 ma/div

I_{CC}, $\overline{RAS}$ ONLY

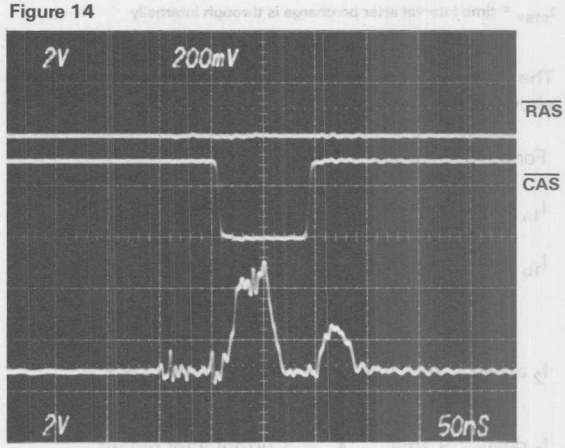
Figure 13



VERTICAL SCALE: 20 ma/div

I_{CC}, PAGE MODE CYCLE

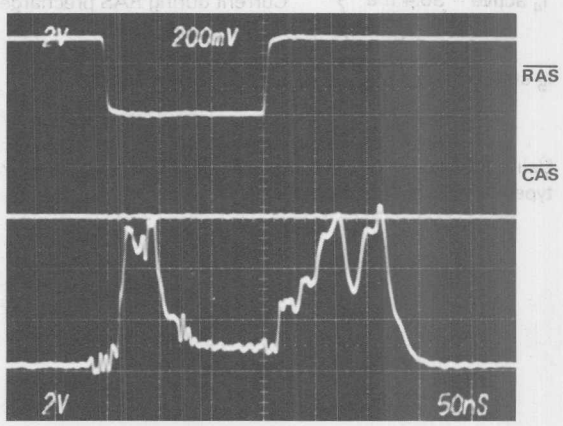
Figure 14



VERTICAL SCALE: 20 ma/div

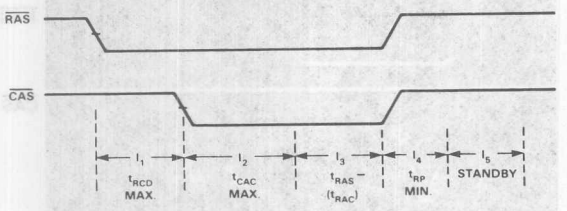
I_{CC}, HIDDEN REFRESH

Figure 15



VERTICAL SCALE: 20 ma/div

III



$$I_{CC} = \frac{I_1\ t_{RCD} + I_2\ t_{CAC} + I_3\ t_{RAS} + I_4\ t_{RP} + I_5\ t_{STBY}}{t_{RC}}$$

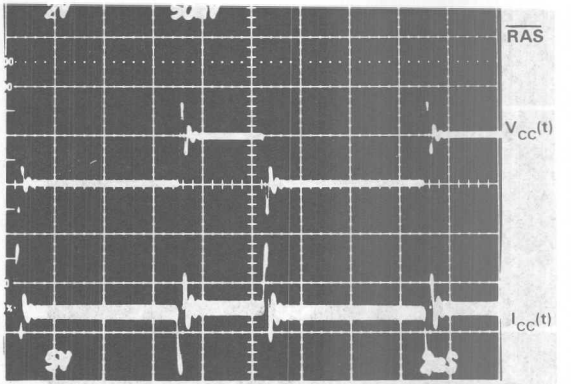
t_{RCD} = $\overline{RAS}$ to $\overline{CAS}$ delay
t_{CAC} = maximum time for valid data to appear on output
$t_{RAS} - t_{RAC}$ = valid data has appeared on output, $\overline{RAS}$ has not gone high
t_{RP} = interval over which precharge is occuring
t_{STBY} = time interval after precharge is through internally

The currents were measured during each time interval as shown on the next page.

For a typical device:

I_{1a} active = 20.3ma	$\overline{RAS}$ to $\overline{CAS}$
I_{1b} delay = 8.5ma after t_{RCD}	I_{1b} is current with $\overline{RAS}$ low and $\overline{CAS}$ high
I_2 active = 24.1 ma	Current when $\overline{CAS}$ comes low
I_3 delay = 9.7ma after t_{CAC}	Current after output is valid but $\overline{CAS}$ and $\overline{RAS}$ still high
I_4 active = 36.4 ma	Current during $\overline{RAS}$ precharge up to t_{RP} min
I_5 standby = 2.6 ma	Current when $\overline{RAS}$ is high

Using these currents, the total average current during any type of cycle can be calculated.

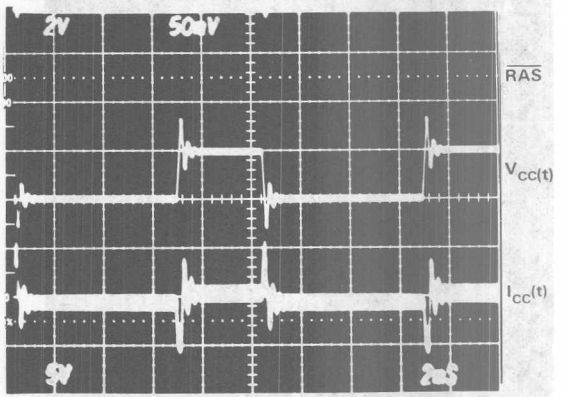


$V_{CC}(t)$ (0 to 5 VOLTS) $I_{CC}(t)$ EMPTY SOCKET

VERTICAL SCALE: 20 ma/div

$I_{CC}(t)$ SHOWN WITH PART IN THE SOCKET

Figure 16b

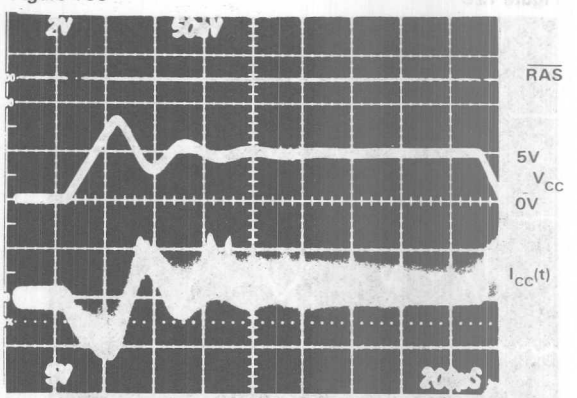


V_{CC} (0 to 5 VOLTS) $I_{CC}(t)$ DEVICE IN SOCKET

VERTICAL SCALE: 20 ma/div

V_{CC} POWER, POWER UP

Figure 16c



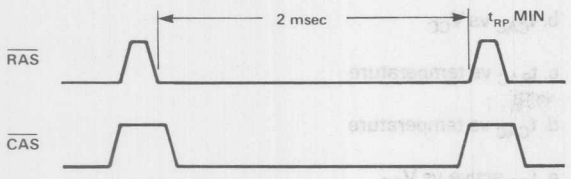
NOTE: DURING V_{CC} POWER UP NO LARGE CURRENT SPIKES ON I_{CC} OCCUR

VERTICAL SCALE: 20 ma/div

I_{CC} STANDBY MEASUREMENTS (TYPICAL) AT T=25°C

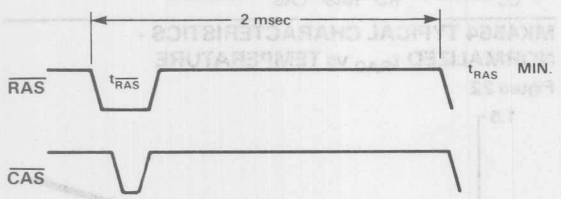
Figure 17

1. Long $\overline{RAS}$ on cycle



$I_{CC} \approx 9.7$ ma

2. Long $\overline{RAS}$ off cycle



$I_{CC} \approx 2.6$ ma

7. INPUT CAPACITANCE

Devices were measured for typical input capacitance values. The technique used for measurement is shown in Figure 19.

Measurements are made first with the device out of the socket so the stray socket capacitance could be subtracted out.

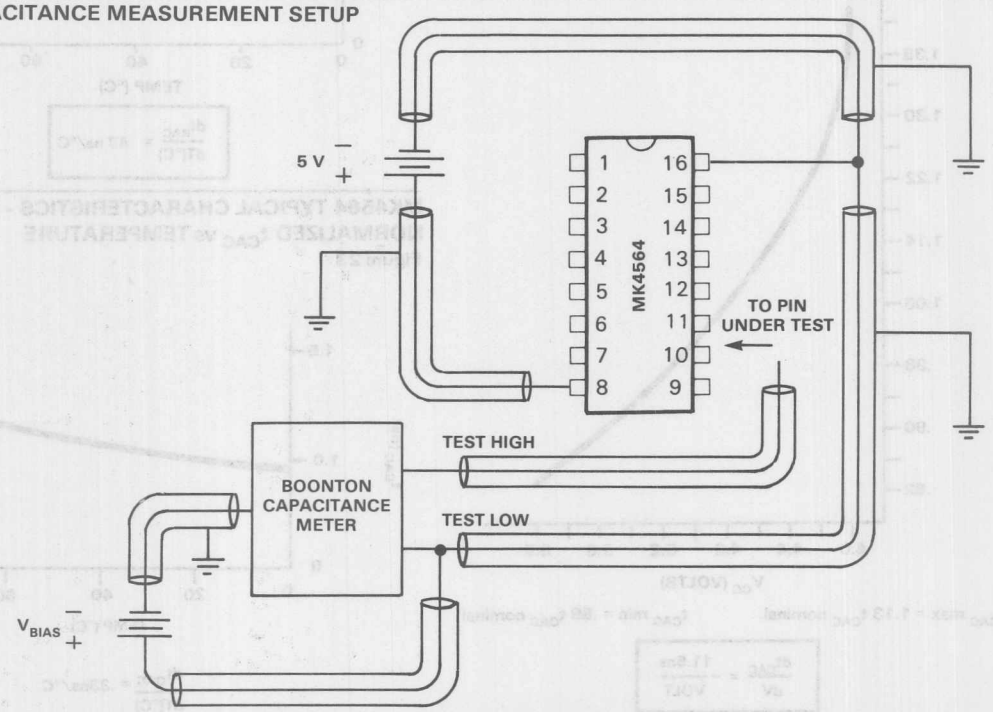
MEASUREMENTS FOR TYPICAL DEVICE IN PLASTIC PACKAGE

Figure 19

Pin #	Function	P-Package	N-Package
1	No connect	1.49	.85
2	D_{IN}	2.16	1.81
3	WE	2.16	1.41
4	RAS	4.65	4.14
5	A0	3.04	2.28
6	A2	2.62	1.94
7	A1	2.12	1.76
9	A7	1.83	1.86
10	A5	2.16	1.79
11	A4	2.45	1.83
12	A3	2.42	1.67
13	A6	4.86	4.35
14	D_{OUT}	6.41	6.38
15	CAS	5.03	5.00

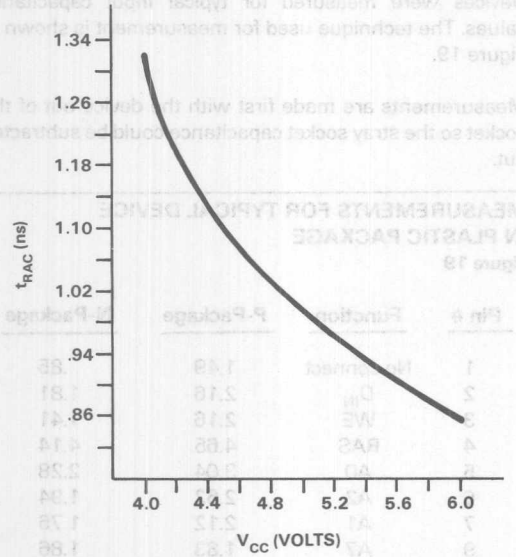
INPUT CAPACITANCE MEASUREMENT SETUP

Figure 18



MK4564 TYPICAL CHARACTERISTICS - t_{RAC} vs V_{CC}

Figure 20

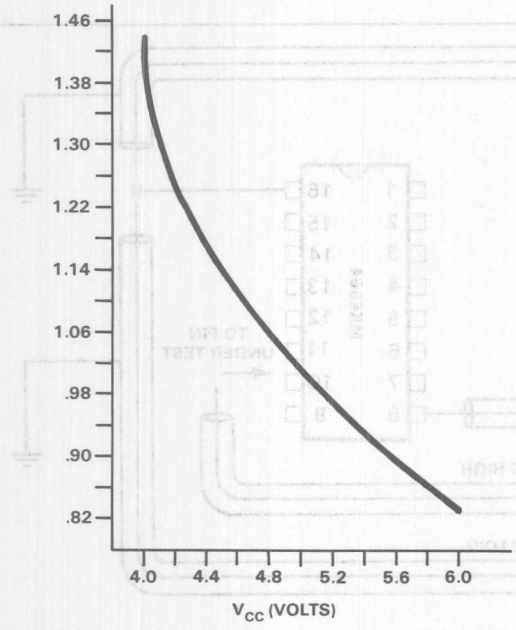


t_{RAC} max. = 1.09 t_{RAC} nominal t_{RAC} min. = .92 t_{RAC} nominal

$$\frac{dt_{RAC}}{dV} = -\frac{17ns}{VOLT}$$

MK4564 TYPICAL CHARACTERISTICS - t_{CAC} vs V_{CC}

Figure 21



t_{CAC} max = 1.13 t_{CAC} nominal t_{CAC} min = .88 t_{CAC} nominal

$$\frac{dt_{CAC}}{dV} = -\frac{11.5ns}{VOLT}$$

8. TYPICAL CHARACTERIZATION DATA

For typical devices graphs are shown for:

a. t_{RAC} vs V_{CC}

b. t_{CAC} vs V_{CC}

c. t_{RAC} vs temperature

d. t_{CAC} vs temperature

e. I_{CC} active vs V_{CC}

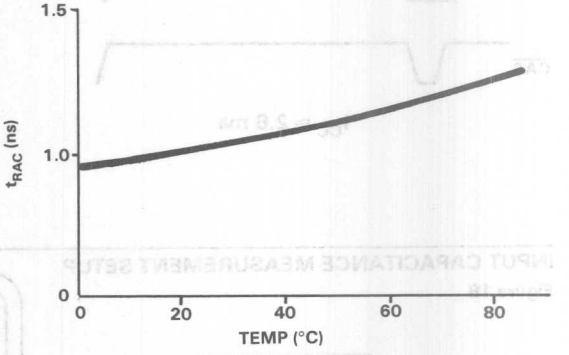
f. I_{CC} standby vs V_{CC}

g. I_{CC} active vs t_{RC}; t_{RP} = constant

h. I_{CC} active vs t_{RC}; t_{RAS}, t_{CAS} = constant

MK4564 TYPICAL CHARACTERISTICS - NORMALIZED t_{RAC} vs TEMPERATURE

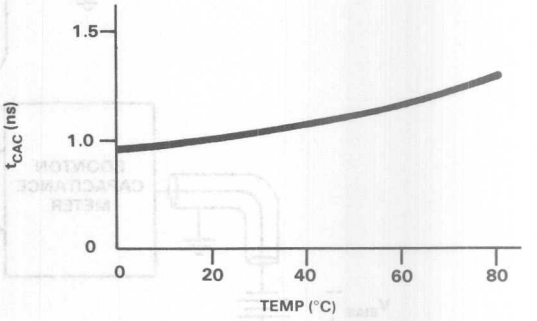
Figure 22



$$\frac{dt_{RAC}}{dT(°C)} = .47\ ns/°C$$

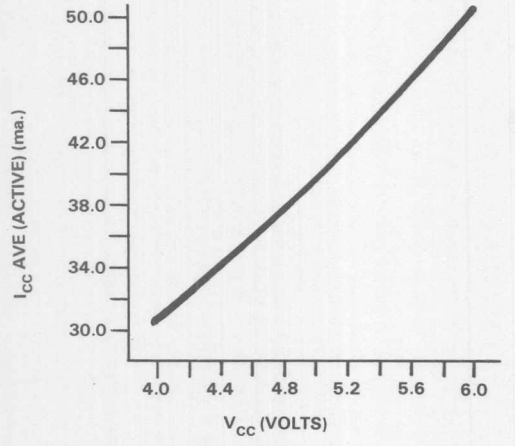
MK4564 TYPICAL CHARACTERISTICS - NORMALIZED t_{CAC} vs TEMPERATURE

Figure 23



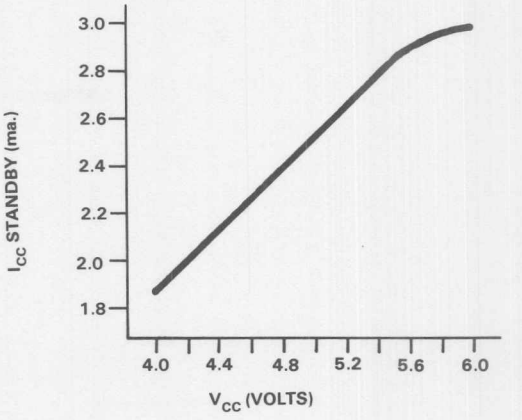
$$\frac{dt_{CAC}}{dT(°C)} = .33ns/°C$$

MK4564 TYPICAL CHARACTERISTICS - I_{CC} ACTIVE vs V_{CC}
Figure 24

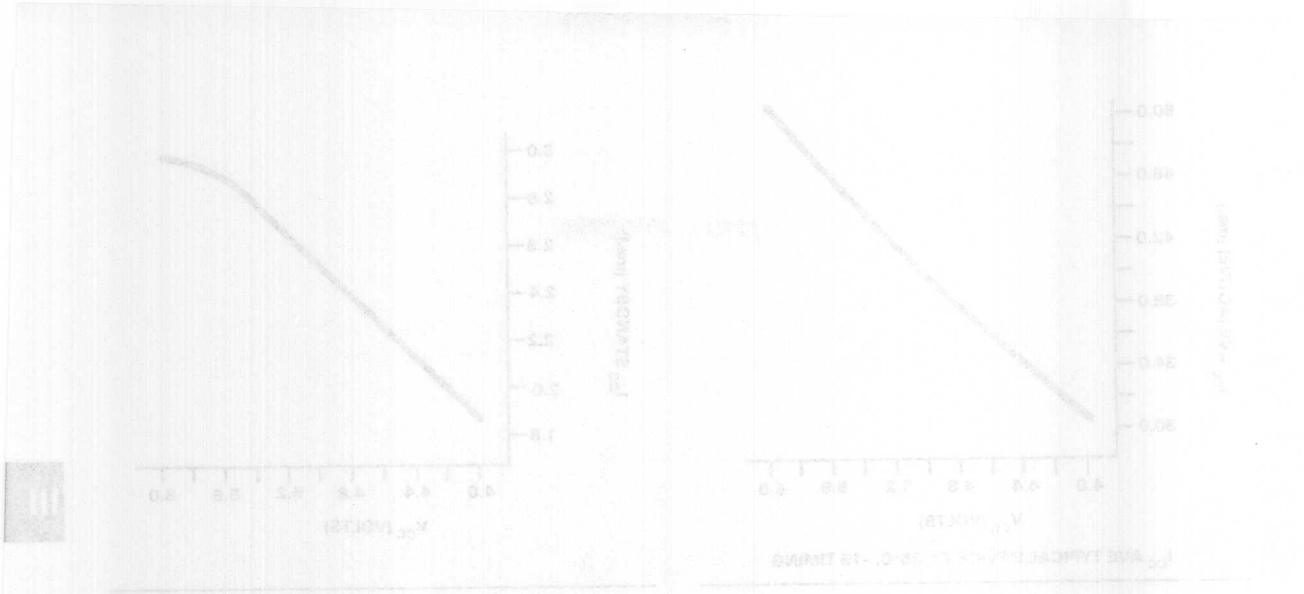


I_{CC} AVE TYPICAL DEVICE T = 25°C, -15 TIMING

MK4564 TYPICAL CHARACTERISTICS - I_{CC} STANDBY vs V_{CC} at 0°C
Figure 25



III



PRINTED CIRCUIT BOARD LAYOUTS
FOR THE COMPATIBLE DYNAMIC RAM FAMILY
Technology Brief

INTRODUCTION

In the past several years dynamic RAMs have dominated the large memory system marketplace. As new RAMs have been introduced, they have forced some users to redesign their memory boards to accommodate the new features and increased density. As a leader in dynamic RAM technology, Mostek has attempted to alleviate this redesign need by introducing a compatibility family concept in the N-bit by 1 dynamic RAM area. As new RAMs are introduced, they are packaged in the same pinout, or in a pinout which is so similar, that the changes between packages are minimized. Thus, increases in the density and function of the RAMs have been incorporated into existing systems without major redesign efforts. Memory systems can be designed to allow the interchange of 4K, 16K, 32K, 64K and 128K bit dynamic RAMs.

The key to the family concept of dynamic RAMs is based on address multiplexing. Mostek pioneered the multiplexed address dynamic RAM with the introduction of a 4096 bit, 16-pin DRAM in 1973. Many members of the memory community felt that multiplexed addressing would not survive. Not only has the multiplexed address DRAM survived, it has become the industry standard for the 16K RAM, as well as for the next generation MK4564, 65536 bit DRAM.

Mostek has extended the address multiplexed dynamic RAM (DRAM) compatible family by offering double density DRAMs by using advanced packaging techniques. The double density DRAMs are constructed by mounting two leadless chip carriers on a single 18 pin substrate. The 18-pin package is pin compatible with its 16-pin counterpart, with the addition of two lower pins for the row and column select controls that access the second chip carrier device. This advanced package concept allows extension of memory density with the current technology devices until the next generation of devices become available and cost effective. When the next generation of devices become available, they can be packaged in a similar manner, to provide even higher density in the double density package. The 16/18-pin compatibility RAM family is shown in Figure 1.

III

MOSTEK'S COMPATIBLE RAM CONCEPT PIN OUT TABLE

Figure 1

4528 128K (5V)	4564 64K (5V)	4516 16K (5V)	4332 32K	4116 16K	4027 4K			4027 4K	4116 16K	4332 32K	4516 16K (5V)	4564 64K (5V)	4528 128K (5V)
			V_{BB}	V_{BB}	V_{BB}	1 (1)	(18) 16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
D_{IN}	D_{IN}	D_{IN}	D_{IN}	D_{IN}	D_{IN}	2 (2)	(17) 15	$\overline{CAS}$	$\overline{CAS}$	$\overline{CAS1}$	$\overline{CAS}$	$\overline{CAS}$	$\overline{CAS1}$
$\overline{WRITE}$	$\overline{WRITE}$	$\overline{WRITE}$	$\overline{WRITE}$	$\overline{WRITE}$	$\overline{WRITE}$	3 (3)	(16) 14	D_{OUT}	D_{OUT}	D_{OUT}	D_{OUT}	D_{OUT}	D_{OUT}
$\overline{RAS1}$	$\overline{RAS}$	$\overline{RAS}$	$\overline{RAS1}$	$\overline{RAS}$	$\overline{RAS}$	4 (4)	(15) 13	$\overline{CS}$	A_6	A_6	A_6	A_6	A_6
A_0	A_0	A_0	A_0	A_0	A_0	5 (5)	(14) 12	A_3	A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2	A_2	6 (6)	(13) 11	A_4	A_4	A_4	A_4	A_4	A_4
A_1	A_1	A_1	A_1	A_1	A_1	7 (7)	(12) 10	A_5	A_5	A_5	A_5	A_5	A_5
V_{CC}	V_{CC}	V_{CC}	V_{DD}	V_{DD}	V_{DD}	8 (8)	(11) 9	V_{CC}	V_{CC}	V_{CC}		A_7	A_7
$\overline{RAS2}$			$\overline{RAS2}$			(9)	(10)			$\overline{CAS2}$			$\overline{CAS2}$

Parentheses Indicate Pin Number of 18 Pin Packages, 16 Pin Devices are Upper Justified in 18 Pin Socket

Differences between the RAMs in this compatible family, as well as techniques for designing memory boards which are useable across the family, will be presented as an aid to designers who are both using present generation dynamic RAMs are planning for future expansion.

The RAMs which will be considered include the following:

MK4116 — 16K Three Supply DRAM
MK4332 — 32K Three Supply DRAM
MK4516 — 16K +5 Volt Only DRAM
MK4564 — 64K +5 Volt Only DRAM
MK4528 — 128K +5 Volt Only DRAM (Double Density MK4564)

Some of these devices are not currently available. They demonstrate the expandibility and memory system design versatility offered by the memory family concept.

Three different compatibility concepts will be discussed to indicate how a memory board can be designed to accommodate different members of the dynamic compatible family, including both the 16-pin and the 18-pin packages. These will be considered as three possible printed circuit layouts as follows:

1. Board compatibility for the three supply members only. These include the MK4116 and the MK4332.

2. Board compatibility for the +5 volt only family members. These include the MK4516, MK4532, MK4564, and the MK4528.

3. Board compatibility for both the single supply (+5 volt) members, as well as the three supply devices, a board design that offers complete compatibility across Mostek's compatible dynamic RAM family.

Multilayer boards to support the different devices are relatively easy to design and will not be discussed. Although many of the recommendations apply to multilayer design, it should be noted that the use of multilayer boards does not preclude the need for careful board layout and circuit/logic design consistent with good engineering practices. Double sided PC boards that will accept numerous members of the compatible family are generally much more difficult to design. However, they are commonly used with dynamic RAMs and can demonstrate adequate margins when properly designed.

In order to design a memory board that is compatible across the complete family or within a subset of the compatible family, it is necessary to understand the fundamental differences between the members of the DRAM family. The five basic areas where the RAMs differ are given below (See Figure 1.):

1. Power supplies — The 16-pin MK4116 and the MK4332 require a three supply power system with +5V, +12, and –5V. The remainder of the RAMs (MK4516, MK4532, MK4164, and the MK4528) require a single +5 volt supply.

2. Addresses — The 16-pin MK4164 (Pin 9) and the 18-pin MK4528 (Pin 11) require an additional address pin to accommodate the increase in RAM density. A7 is used for this purpose. This pin is a N/C (No Connect, Not Bonded) on the MK4516/MK4532 and is used for V_{CC} (+5 volts) on the MK4116/MK4332.

3. $\overline{RAS}$ and $\overline{CAS}$ — The double density packages (MK4332, MK4532 and the MK4528) require an additional $\overline{RAS}/\overline{CAS}$ pair (Pins 9 and 10) of strobe signals to select the second chip on the package. These are connected to the extra two pins located at the lower end of the package.

4. V_{CC} Location — The single +5 volt parts have V_{CC} connection on a different pin than the three supply parts. In actuality, the primary power pin (Drain Supply) has remained unchanged, but the supply requirement has changed from +12 volts to +5 volts.

MK4116/MK4332 Compatible Board Layout

The layout shown in Figure 2 has been used successfully with both the older 4096 bit RAM, the MK4096/MK4027 and the 16K RAM, the MK4116. If the user has experience with this layout and confidence in using it, it is possible to modify it to accept the double density MK4332 DRAM. Two additional pins must be added to the lower end of each device site to provide the additional $\overline{RAS}$ and $\overline{CAS}$ strobe signals required to select the second half of the double density package.

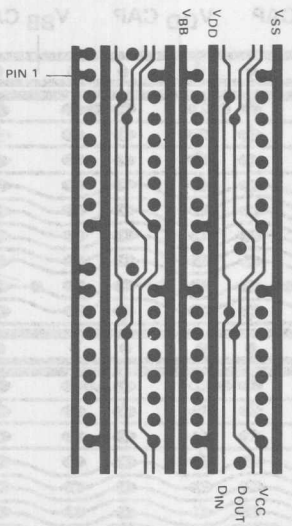
Note that the additional $\overline{RAS}$ and $\overline{CAS}$ strobe signals do not require an increase in the vertical spacing (300 Mils) between the rows of RAMs even though the bottom two pins are used for signal traces instead of power. The vertical spacing can remain at 300 Mils as previously shown with the 16-pin layout. However, the 18-pin layout does require .05 square inches more area per RAM than required with the 16-pin layout.

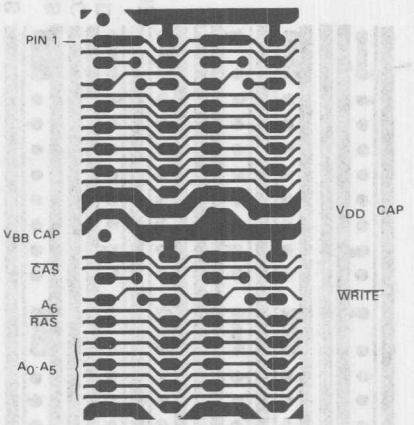
The 18 pin version of basic layout shown in Figure 2 can be modified to eliminate the geometric complexity of the metal traces. The simplified layout is shown in Figure 3. The capacitors have been relocated to the center of the horizontal power bus channel and have been aligned directly above the memory devices. This arrangement allows the use of capacitors with either 300 Mil or 200 Mil lead spacing. For 300 Mil spacing, the caps are inserted directly above the IC locations (See Figure 4A) and for 200 Mil lead spacing, the caps are inserted above the spacing between the IC locations (See Figure 4B). The relocation of the capacitors simplifies the routing of the vertical signals and the power traces and permits auto-insertion of the capacitors within the memory array matrix.

Figures 5 and 6 show the suggested MK4116/MK4332 compatible PCB layouts. These layouts are slight modifications of the layout shown in Figure 3. The vertical power bussing has been routed down the 300 Mil spacing under the IC and the data-in and data-out lines have been routed down

18 PIN MK4116/MK4332 COMPATIBLE LAYOUT

Figure 2



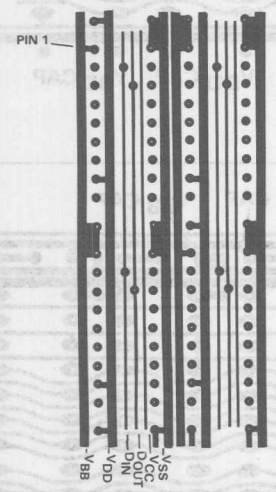


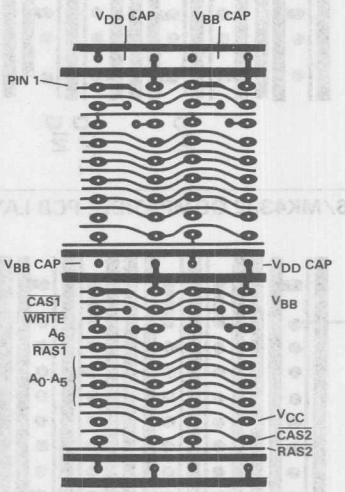
Frequently used layout for 16 pin 3 supply address multiplexed Dynamic RAMs

III

(SIMPLIFICATION OF 18 PIN LAYOUT)

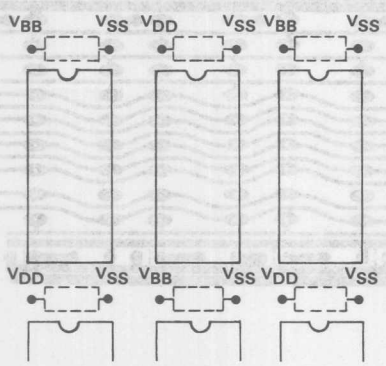
Figure 3





CAPS PLACED ON 300 MIL SPACING

Figure 4A



CAPS PLACED ON 200 MIL SPACING

Figure 4B

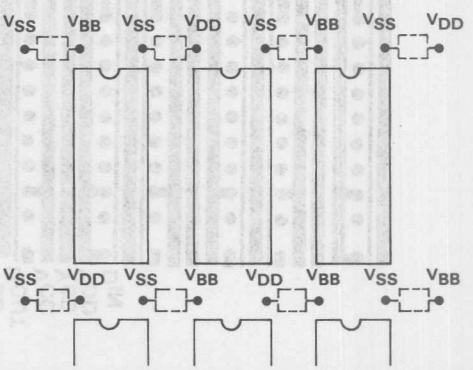
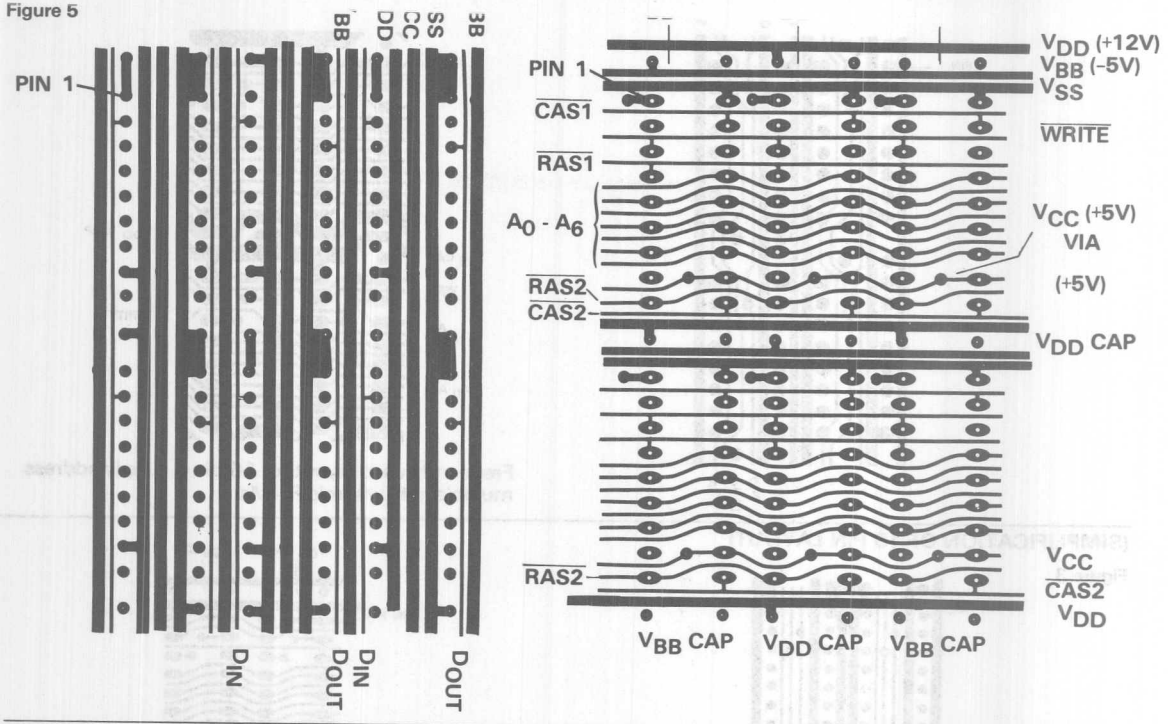
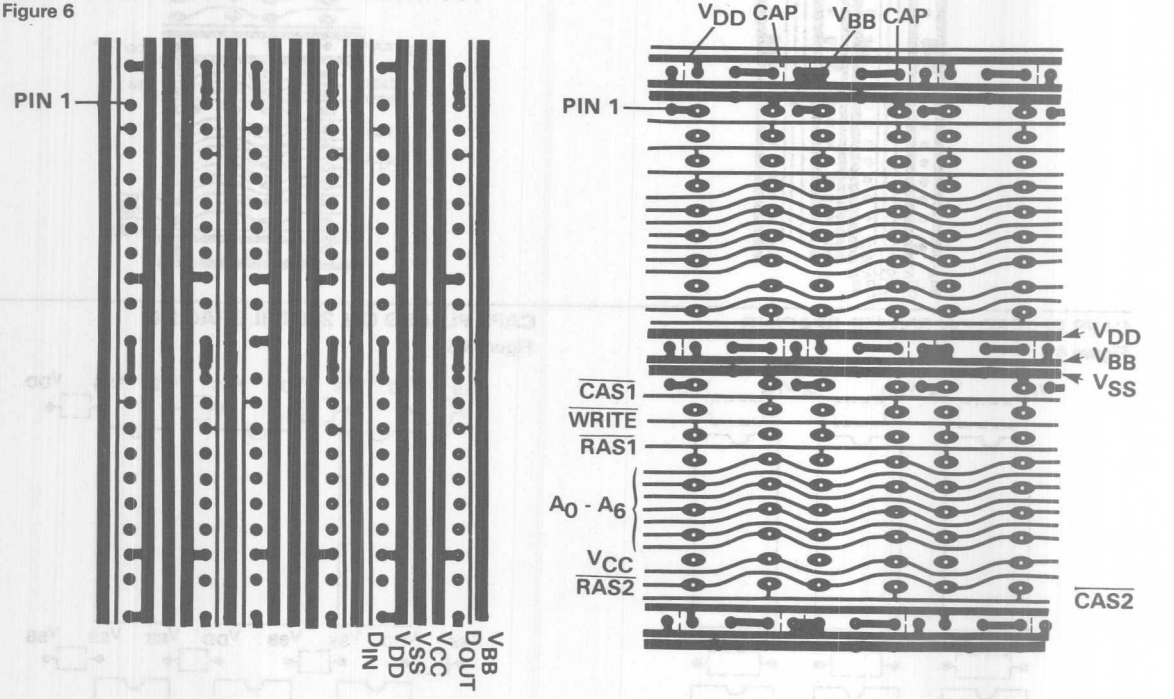


Figure 5



MK4116/MK4332 COMPATIBLE PCB LAYOUT

Figure 6



running a decoupled supply or ground trace between them. The data-out to data-in coupling is generally not a problem, except during late write cycles where transitions on the data-out line can cause perturbations on the data-in line if sufficient coupling between the two lines exists. This condition may cause a violation of either data-in setup times or data-in hold times during the write cycle. In most cases, this problem can be avoided by using time discrimination.

The layout shown in Figure 5 is preferred due to the direct V_{DD} and V_{SS} to the RAM pins and the decoupling capacitors. Furthermore, the simplicity of the layout is very attractive. However, it does have the disadvantage of having a V_{CC} (+5 volt) VIA (Feed Through) under all RAM packages. The layout shown in Figures 2, 3 and 5 also have the VIAs under the RAMs. If feed throughs under ICs are prohibited in your design, Figure 7 shows a MK4116/MK4332 layout which eliminates them.

When using the layouts shown in Figures 3, 5, or 6 with the MK4116, the following considerations apply:

When using the layouts shown in Figures 3, 5, or 6 with the MK4332, these considerations apply:

1. The 18-pin devices are inserted directly into the 18-pin sites.

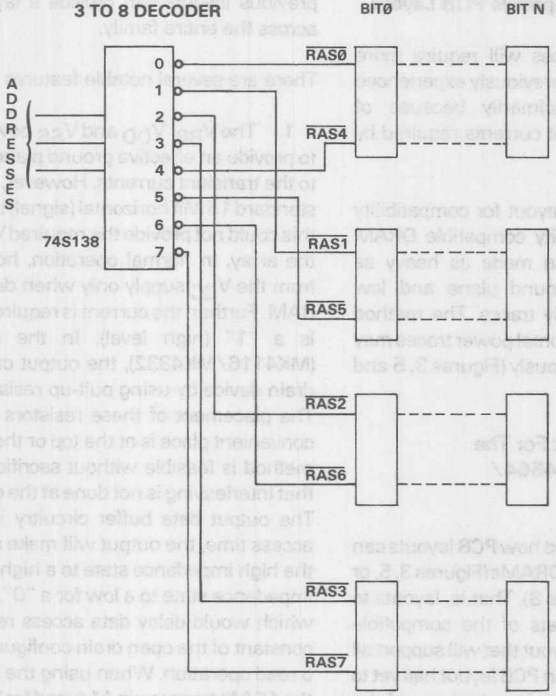
2. Since the 16K address boundary requirements for the MK4332 RAS decoding are identical to that for the MK4116, no major modifications are required for complete compatibility. The extra $\overline{RAS}$ and $\overline{CAS}$ inputs must be provided, based on 16K boundaries. This addition does not generally require jumper wires to handle the $\overline{RAS}$ clocks. Figure 8 illustrates a method which can be used to avoid jumper wires in the $\overline{RAS}$ decoding logic. However, jumpers or switches are usually needed to adjust the board selection logic such that the memory subsystem acknowledges and responds to changes in memory density.

3. The power supply must provide the additional current needed to support the double density 32K devices.

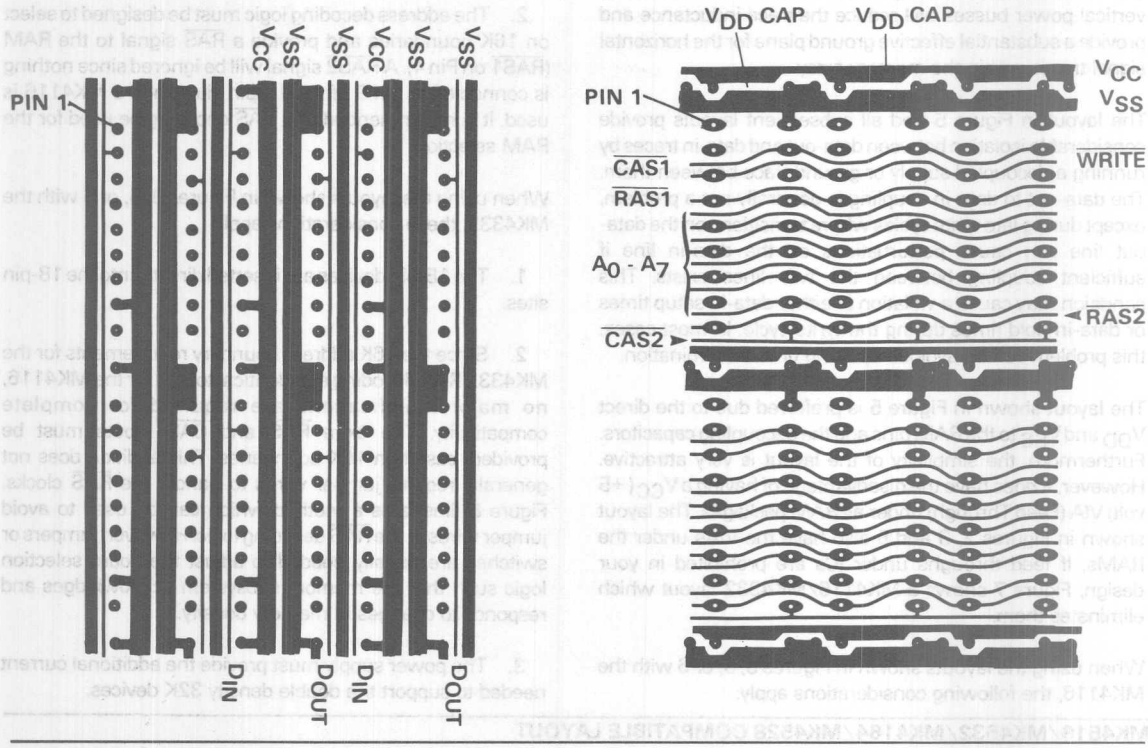
III

MK4516/MK4532/MK4164/MK4528 COMPATIBLE LAYOUT

Figure 7



MK4516/MK4532/MK4164/MK4528 COMPATIBLE LAYOUT
Figure 8



MK4516/MK4564/MK4528 Compatible PCB Layout

The use of the single +5 volt devices will require more demanding design efforts than those previously experienced with the three supply devices, primarily because of considerations due to higher transient currents required by the +5 volt only devices.

Figure 8 shows the suggested PCB layout for compatibility across the single +5 volt high density compatible DRAM family. The power bussing has been made as heavy as possible to provide an effective ground plane and low inductance in the array power supply traces. The method used in Figure 8 to "beef up" the horizontal power traces may be used with the layouts shown previously (Figures 3, 5 and 6).

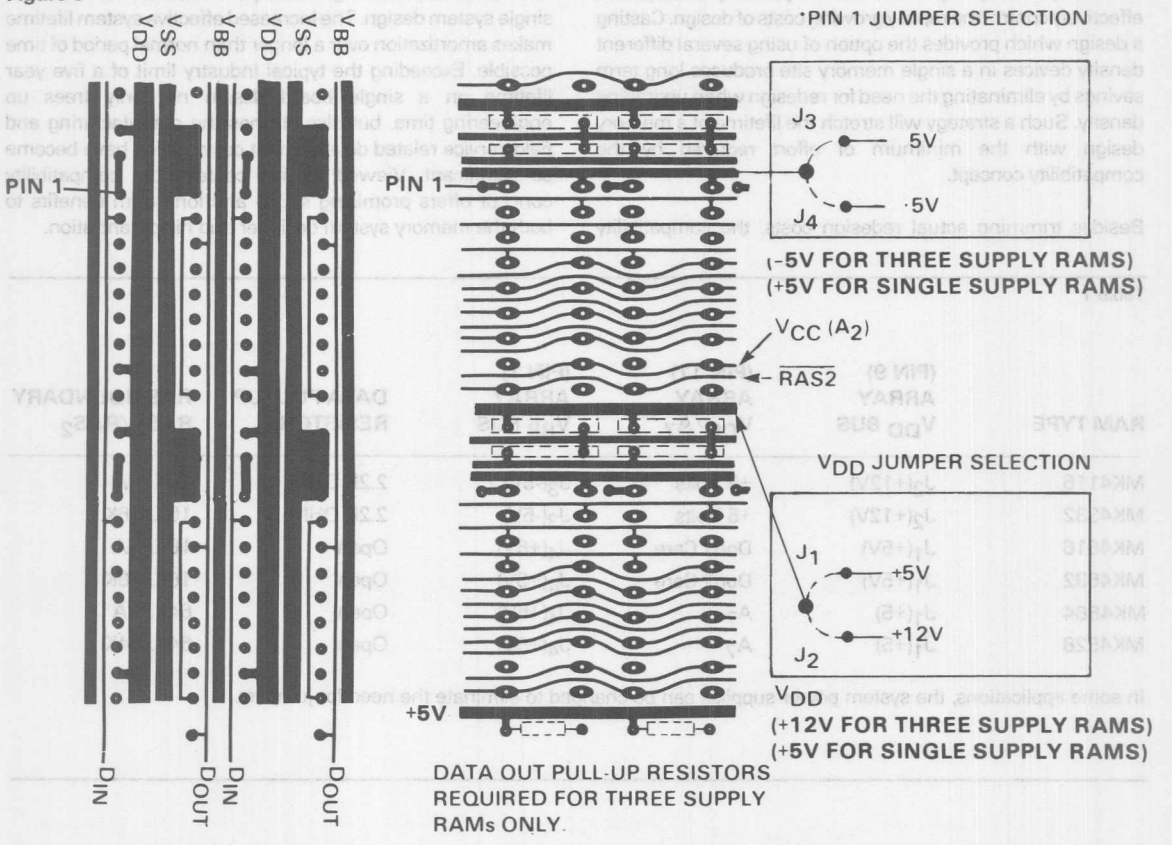
Complete Compatible Board Layout For The MK4116/MK4332/MK4516/MK4564/MK4528

The previous examples have suggested how PCB layouts can accommodate either the three supply DRAMs (Figures 3, 5, or 6) or the single +5 volt devices (Figure 8). That is, layouts to support one of the two basic subsets of the compatible DRAMs have been discussed, but a layout that will support all of the compatible devices on a common PCB layout has yet to be proposed. Figure 9 shows how the best features of the previous layouts can provide a layout for full compatibility across the entire family.

There are several notable features of this layout:

1. The V_{BB}, V_{DD} and V_{SS} power busses are very wide, to provide an effective ground plane and to reduce noise due to the transient currents. However, V_{CC} is provided by only a standard 15 Mil horizontal (signal) trace. Normally, the size of this could not provide the required V_{CC} level to the devices in the array. In normal operation, however, current is drawn from the V_{CC} supply only when data is being read from the RAM. Further, the current is required only when the data-out is a "1" (high level). In the multiple supply devices (MK4116/MK4332), the output can be treated as an open drain device by using pull-up resistors on the data-out port. The placement of these resistors is non-critical. The most convenient place is at the top or the bottom of the array. This method is feasible without sacrificing access time provided that interleaving is not done at the chip level within the array. The output data buffer circuitry is designed such that, at access time, the output will make a monotonic change from the high impedance state to a high for a "1" or from the high impedance state to a low for a "0". That is, glitches or spikes which would delay data access resulting from the RC time constant of the open drain configuration, do not occur during a read operation. When using the MK4116 or the MK4528, the 15 Mil trace to pin 11 (used for V_{CC} with the three supply

Figure 9



devices) becomes the A7 address line. If the MK4516 is used, this input does not function and may be allowed to "float". However, it is recommended that it be tied to a high or a low level to reduce noise within the array.

2. If the array layout has space limitations, the horizontal ground gridding at the bottom of the array may be excluded when interface circuits or critical ground current paths below the array do not exist. When eliminated, the power busses, including ground, should be extended under the bottom device to provide the ground plane effect for the signals to the bottom devices. (See Figure 9.)

3. The second $\overline{CAS}$ ($\overline{CAS2}$ on Pin 10) line for the double density devices is tied to the original $\overline{CAS}$ line ($\overline{CAS1}$, Pin 17). This configuration is acceptable if $\overline{RAS}$ decoding selection is done. Experience has shown that such short stubbing has very little effect on the $\overline{CAS}$ signal waveform. If $\overline{CAS}$ decoding is used, then the additional $\overline{CAS2}$ line must be routed through the array as shown in the previous layouts.

4. "$\overline{RAS}$-Only" refresh must be used with this layout, even with the single +5 volt devices, because pin 1 is tied to the V_{BB} gridding, which is required for the three supply RAMs. Therefore, for proper operation, pin 1 trace must be tied high (resistor to +5 volts or direct connection to +5 volts) when using the single supply devices.

5. When the single supply devices are used, all of the decoupling capacitors connected to the drain supply (V_{CC}) should be installed. One cap for every other device is an absolute minimum. The V_{BB} capacitors do not have to be installed when using the single supply devices.

The DRAM family compatible PCB layout shown in Figure 9 can be used with any of the Mostek 16-pin or 18-pin high density (N-bit by 1 organization) dynamic RAMs. Table 1 summarizes the array conditions required for each RAM type when using the compatible layout (Figure 9).

Conclusion

A PCB memory matrix layout suitable for use with any of the Mostek compatible family of high density RAM devices has been shown. Minor jumper type changes allow the versatility associated with this compatibility concept. Because the designer may wish to employ only one part of the DRAM family, layouts tailored for each of the family's two major subsets (three power supply devices versus one supply) were also described.

a design which provides the option of using several different density devices in a single memory site produces long term savings by eliminating the need for redesign when upgrading density. Such a strategy will stretch the lifetime of a memory design with the minimum of effort required by the compatibility concept.

Besides trimming actual redesign costs, the compatibility makes amortization over a longer than normal period of time possible. Exceeding the typical industry limit of a five year lifetime on a single board design not only frees up engineering time, but also slashes the manufacturing and field service related development costs which have become so significant. Viewed in this context, the compatibility concept offers promising short- and long-term benefits to both the memory system designer and his organization.

Table 1

RAM TYPE	(PIN 9) ARRAY V_{DD} BUS	(PIN 11) ARRAY V_{CC}/A_7	(PIN 1) ARRAY V_{BB} BUS	DATA PULL-UP RESISTORS	RAS BOUNDARY RAS_1/RAS_2
MK4116	J_2(+12V)	+5 Volts	J_3(-5V)	2.2K OHM	16K/NA
MK4332	J_2(+12V)	+5 Volts	J_3(-5V)	2.2K OHM	16K/16K
MK4516	J_1(+5V)	Don't Care	J_4(+5V)	Open	16K/NA
MK4532	J_1(+5V)	Don't Care	J_4(+5V)	Open	16K/16K
MK4564	J_1(+5)	A_7	J_4(+5V)	Open	64K/NA
MK4528	J_1(+5)	A_7	J_4(+5V)	Open	64K/64K

In some applications, the system power supplies can be changed to eliminate the need for jumpers.

MK4564 TOPOLOGICAL CONSIDERATIONS

Application Note

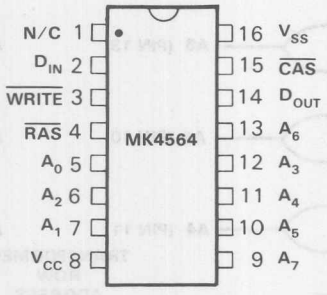
This application note describes the internal topology and address transformation for the Mostek MK4564, 65,536 bit dynamic RAM such that the task of device evaluation or characterization can be approached in a systematic fashion. Futhermore, the information disclosed is useful in determining "worst case" patterns and developing optimized test sequences.

EXTERNAL ADDRESS DEFINITION

Sixteen address bits are required to select the 65,536 unique cell locations. The MK4564 uses only eight address inputs in a timeshared scheme such that eight addresses are entered when $\overline{RAS}$ (Row Address Strobe) goes low and the additional eight addresses are entered when $\overline{CAS}$ (Column Address Strobe) goes low. These eight address inputs to the MK4564 are designated A0 through A7 as shown in the pin out diagram in Figure 1. Since the order of significance associated with A0 through A7 is different during row and column time (see Row/Column address transformation information), A0 (Pin 5) is assigned the least significant bit with ascending binary weights such that A7 (Pin 9) is the most significant bit. This address definition will be used throughout the application note.

PIN OUT

Figure 1



PIN FUNCTIONS

A_0 - A_7	Address Inputs	$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe	$\overline{WRITE}$	Read/ Write Input
D_{IN}	Data In	N/C	Not Connected
D_{OUT}	V_{CC}	Power (+5 V)	
		V_{SS}	GND

The addresses applied directly to the device (A0 through A7) will be referred to as "external" addresses. For the reader's convenience, the external addresses are given in decimal, binary, and hexadecimal representations.

INTERNAL ADDRESS DEFINITION

Efficient layout of the row and column decoders results in a scramble of the address inputs which must be compensated for if the internal rows and columns are to be accessed in a desired sequence when testing the MK4564 for nearest neighbor effects or other address/data pattern sensitivities. Figure 2 describes the device topology. There is an orderly arrangement of 256 rows, ROW 0 through ROW 255, and 256 columns, COL 0 through COL 255. "Internal" addresses will be used to identify these internal row and column locations. The internal addresses are given in decimal.

ROW/COLUMN ADDRESS TRANSFORMATION

Figure 3 shows the logical address transformation required to compensate for the internal (on-chip) row address scrambling. A0 (LSB) through A7 (MSB) are the external address bits presented to the chip during row address time as previously mentioned. R0 (LSB) through R7 (MSB) form the external address field used for the row addresses.

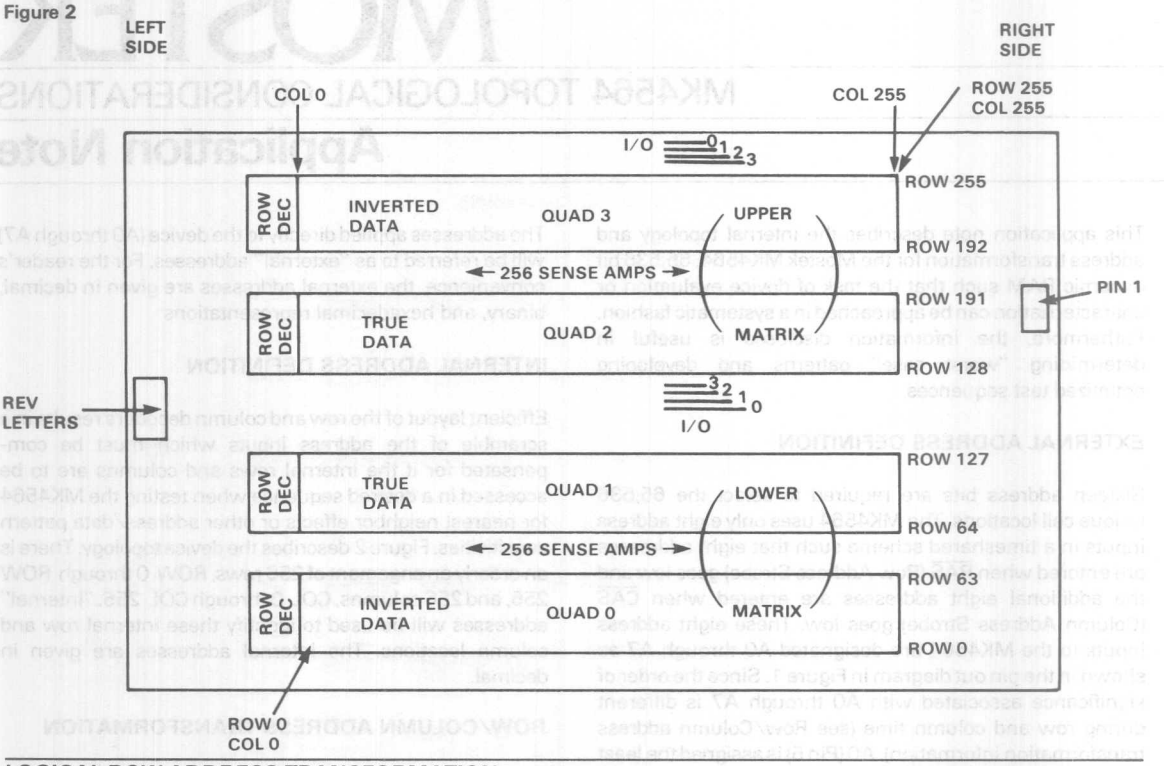
Figure 4 shows the logical address transformation required to compensate for the internal (on-chip) column address scrambling. A0 (LSB) through A7 (MSB) are the external address bits presented to the chip during column address time. C0 (LSB) through C7 (MSB) form the external address field used for the column addresses.

The row address transformation shown in Figure 3 results in a direct relationship between R0 through R7 and the internal ROW 0 through ROW 255; the equivalent of the desired internal row location (input to the row transformation) will address that internal row within the device. If, for example, R0 through R7 address field is sequentially incremented from all zeros to all ones, then the internal row locations 0 through 255 would have been accessed in an ascending sequential fashion. Likewise, with the column address transformation shown in Figure 4, a direct relationship exists between C0 through C7 and the internal columns.

Note that the true order of significance for A0 through A7 at row time can be seen by inspecting the relationships

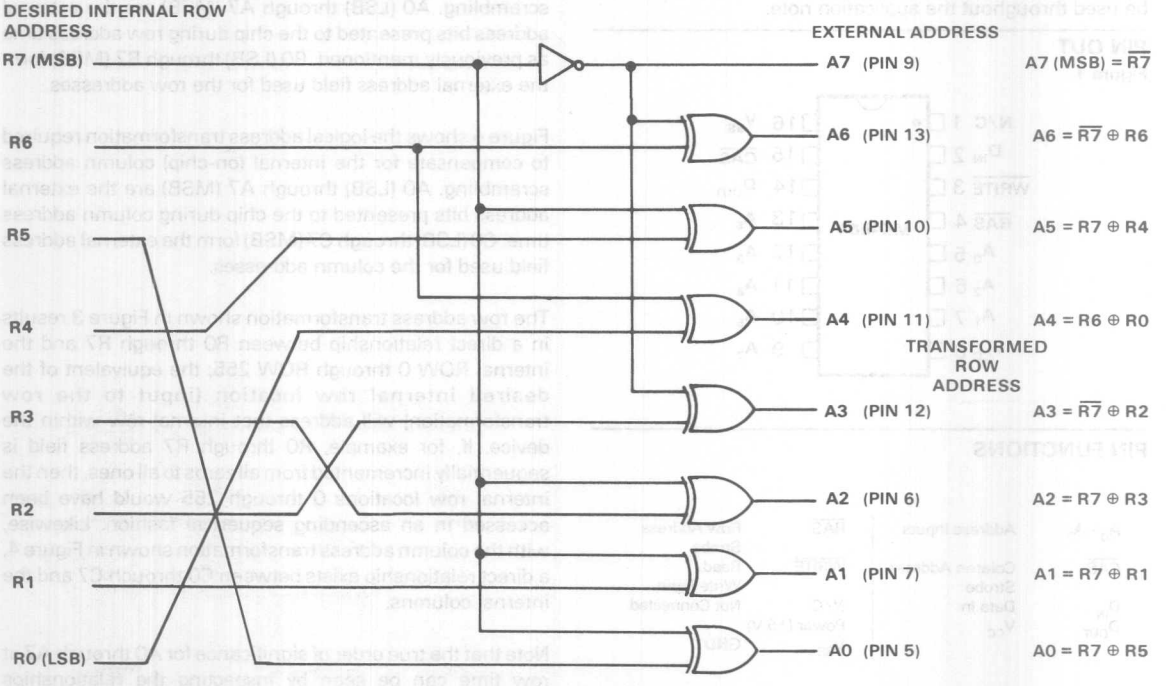
DEVICE TOPOLOGY

Figure 2



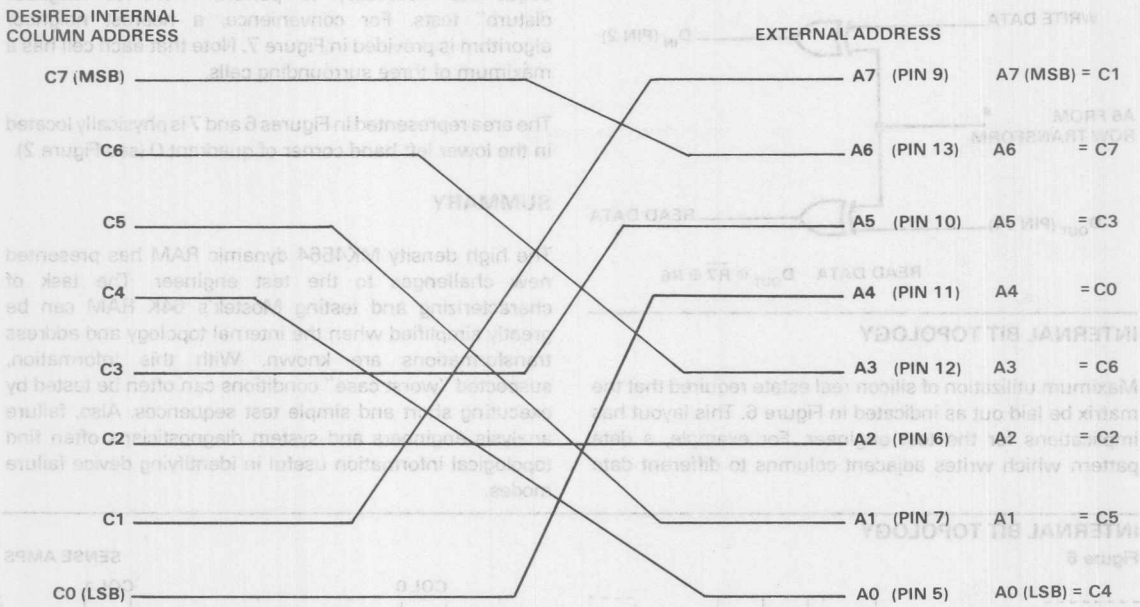
LOGICAL ROW ADDRESS TRANSFORMATION

Figure 3



LOGICAL COLUMN ADDRESS TRANSFORMATION

Figure 4



between the row transform input addresses and the transform output addresses (external addresses). A similar analysis of the column transform will reveal the true bit significance for the column external addresses. See Figures 3 and 4.

The use of logical gates as previously illustrated is not the only method of performing the address interpolation. Many testers use ROMs or software modifiable address scrambling circuits to perform the transform function via a mapping technique. When using these mapping techniques, it is more convenient to have the address transformation presented in a numerical format. The address transformations are provided in a numerical form in Tables 1 and 2; Table 1 describes the row address transformation and Table 2 provides the column address transformation.

"RAS-ONLY" REFRESH CONSIDERATIONS WHEN USING ROW ADDRESS TRANSFORMATIONS

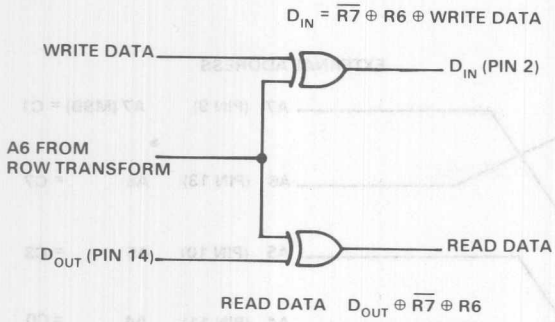
The MK4564 ignores the most significant row address (A7) during a refresh cycle. However, if an external address transformation is used, care must be exercised to insure that all 128 row address combinations are cycled each 2 milliseconds. Even though A7 is not required during "RAS-only" refresh cycles, ignoring the logical state of this address when using the address transformation can result in a violation of this refresh requirement. Both the logical representation of the row transformation shown in Figure 3 and the numerical form shown in Table 1 disclose the problem. Each time R7 changes state, a break in the binary address sequence occurs. Since the order of addressing is altered, the 128 cycle/2 ms refresh requirement may not be met. This effect can be eliminated by "forcing" R7 to a fixed state for all refresh cycles, refreshing more frequently to compensate for the increased number of refresh cycles needed during each 2 millisecond interval, or simply bypassing the row transformation during refresh cycles.

DATA POLARITY

Figure 2 shows that the 64K array is organized as two 32K sub-matrices utilizing balanced sense amplifiers between ROWS 63 and 64 in the lower matrix and between ROWS 191 and 192 in the upper matrix. This requires that one side of each matrix actually stores inverted data, as illustrated in Figure 2. The data inversion is completely transparent to the user. However, if one wishes to store a "true" data pattern in the RAM such that all locations are in the charged (or discharged) state, it is necessary to invert the data when writing into quad 0 and quad 3 (see Figure 2).

The logical transformation necessary to counteract the internal inversion of data with the MK4564 is shown in Figure 5.

Figure 5



INTERNAL BIT TOPOLOGY

Maximum utilization of silicon real estate required that the matrix be laid out as indicated in Figure 6. This layout has implications for the test engineer. For example, a data pattern which writes adjacent columns to different data topology is also helpful in determining addressing sequences necessary to perform "nearest neighbor disturb" tests. For convenience, a nearest neighbor algorithm is provided in Figure 7. Note that each cell has a maximum of three surrounding cells.

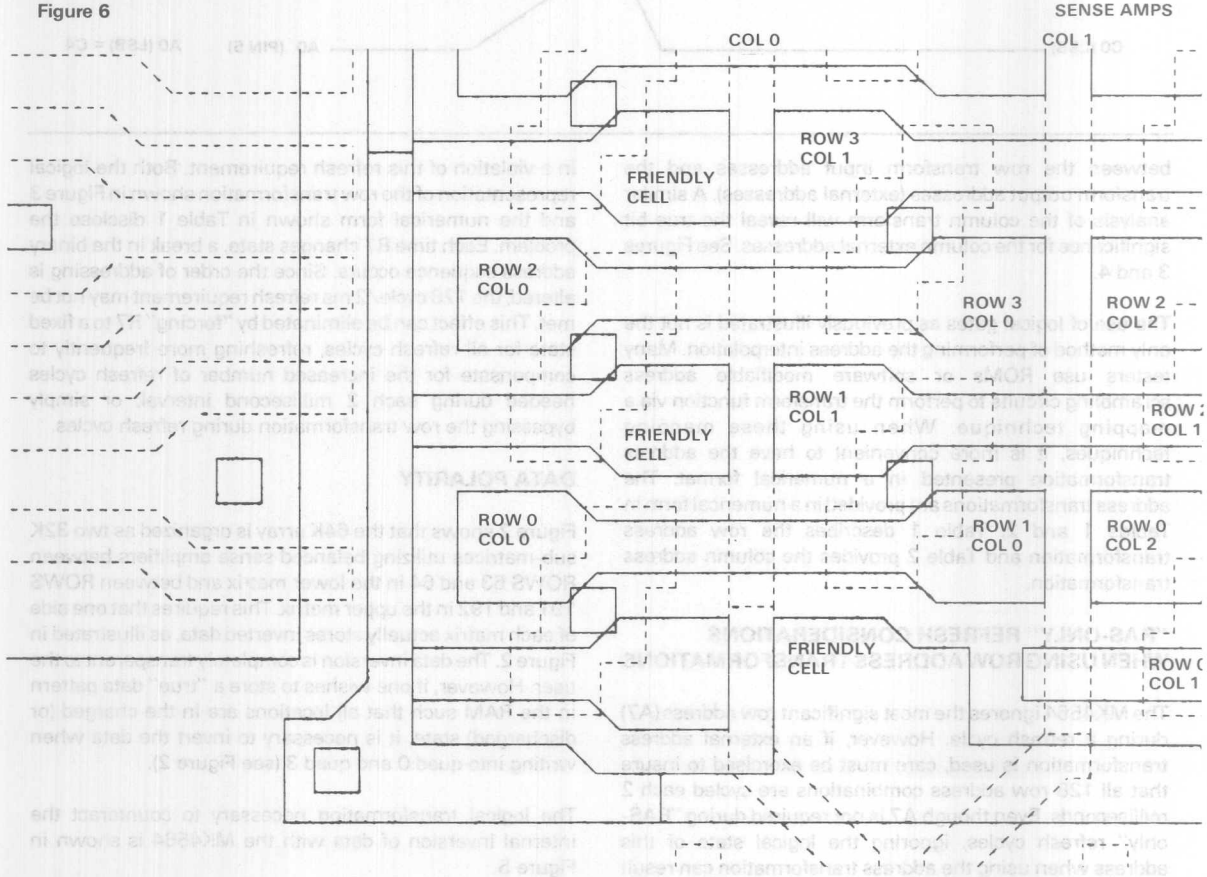
The area represented in Figures 6 and 7 is physically located in the lower left hand corner of quadrant 0 (see Figure 2).

SUMMARY

The high density MK4564 dynamic RAM has presented new challenges to the test engineer. The task of characterizing and testing Mostek's 64K RAM can be greatly simplified when the internal topology and address transformations are known. With this information, suspected "worst case" conditions can often be tested by executing short and simple test sequences. Also, failure analysis engineers and system diagnosticians often find topological information useful in identifying device failure modes.

INTERNAL BIT TOPOLOGY

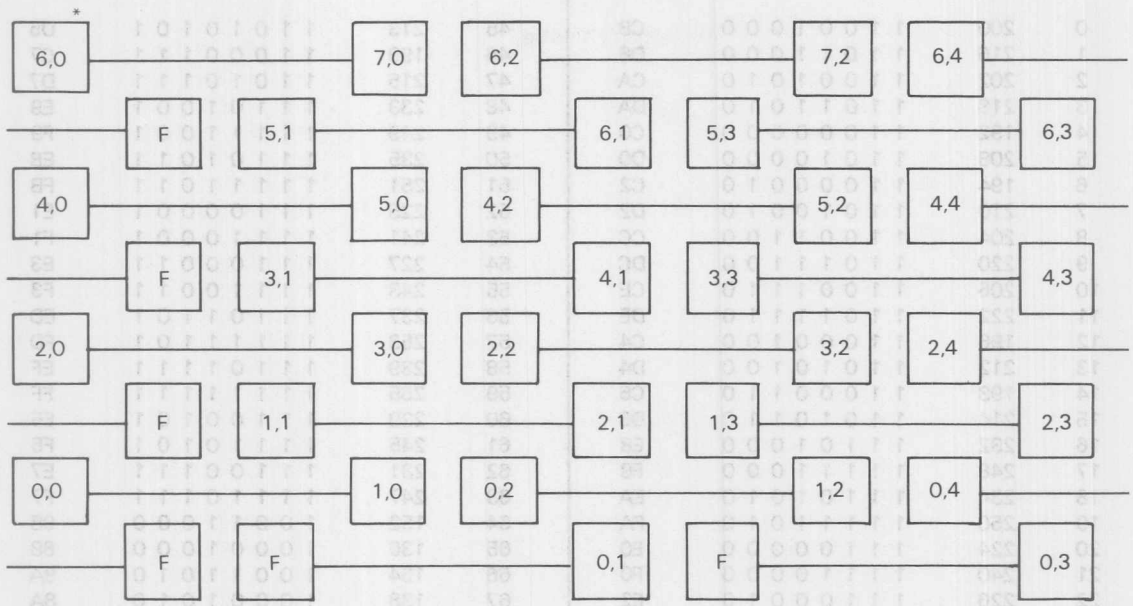
Figure 6



NEAREST NEIGHBOR ALGORITHM

Figure 7

1. Each cell has 3 nearest neighbors as shown below:



2. To find the nearest neighbors, use the following algorithm.

Row	If i and j are either both odd or both even, then the nearest cells have rows i+2, i+1, i If i and j are not both odd or even, then the nearest cells have rows i, i-1, i-2
Column	If i and j are either both odd or both even, the nearest cells have columns j-1, j-2, j-1 If i and j are not both odd or even the nearest cells have columns j+1, j+2, j+1

EXAMPLES:

NEAREST NEIGHBORS				
	2,4	3,2	5,3	6,3
	4,3	3,3	7,2	6,4
	3,2	2,4	6,1	5,5
	2,3	1,3	5,2	4,4

*Location identified
By ROW, COLUMN OR i, j.

III

MK4564 TOPOGRAPHICAL MAP ROW ADDRESS RELATIONSHIPS

Table 1

Internal Dec.	External Dec.	External Binary	External Hex	Internal Dec.	External Dec.	External Binary	External Hex
0	200	1 1 0 0 1 0 0 0	C8	45	213	1 1 0 1 0 1 0 1	D5
1	216	1 1 0 1 1 0 0 0	D8	46	199	1 1 0 0 0 1 1 1	C7
2	202	1 1 0 0 1 0 1 0	CA	47	215	1 1 0 1 0 1 1 1	D7
3	218	1 1 0 1 1 0 1 0	DA	48	233	1 1 1 0 1 0 0 1	E9
4	192	1 1 0 0 0 0 0 0	C0	49	249	1 1 1 1 1 0 0 1	F9
5	208	1 1 0 1 0 0 0 0	D0	50	235	1 1 1 0 1 0 1 1	EB
6	194	1 1 0 0 0 0 1 0	C2	51	251	1 1 1 1 1 0 1 1	FB
7	210	1 1 0 1 0 0 1 0	D2	52	225	1 1 1 0 0 0 0 1	E1
8	204	1 1 0 0 1 1 0 0	CC	53	241	1 1 1 1 0 0 0 1	F1
9	220	1 1 0 1 1 1 0 0	DC	54	227	1 1 1 0 0 0 1 1	E3
10	206	1 1 0 0 1 1 1 0	CE	55	243	1 1 1 1 0 0 1 1	F3
11	222	1 1 0 1 1 1 1 0	DE	56	237	1 1 1 0 1 1 0 1	ED
12	196	1 1 0 0 0 1 0 0	C4	57	253	1 1 1 1 1 1 0 1	FD
13	212	1 1 0 1 0 1 0 0	D4	58	239	1 1 1 0 1 1 1 1	EF
14	198	1 1 0 0 0 1 1 0	C6	59	255	1 1 1 1 1 1 1 1	FF
15	214	1 1 0 1 0 1 1 0	D6	60	229	1 1 1 0 0 1 0 1	E5
16	232	1 1 1 0 1 0 0 0	E8	61	245	1 1 1 1 0 1 0 1	F5
17	248	1 1 1 1 1 0 0 0	F8	62	231	1 1 1 0 0 1 1 1	E7
18	234	1 1 1 0 1 0 1 0	EA	63	247	1 1 1 1 0 1 1 1	F7
19	250	1 1 1 1 1 0 1 0	FA	64	152	1 0 0 1 1 0 0 0	98
20	224	1 1 1 0 0 0 0 0	E0	65	136	1 0 0 0 1 0 0 0	88
21	240	1 1 1 1 0 0 0 0	F0	66	154	1 0 0 1 1 0 1 0	9A
22	226	1 1 1 0 0 0 1 0	E2	67	138	1 0 0 0 1 0 1 0	8A
23	242	1 1 1 1 0 0 1 0	F2	68	144	1 0 0 1 0 0 0 0	90
24	236	1 1 1 0 1 1 0 0	EC	69	128	1 0 0 0 0 0 0 0	80
25	252	1 1 1 1 1 1 0 0	FC	70	146	1 0 0 1 0 0 1 0	92
26	238	1 1 1 0 1 1 1 0	EE	71	130	1 0 0 0 0 0 1 0	82
27	254	1 1 1 1 1 1 1 0	FE	72	156	1 0 0 1 1 1 0 0	9C
28	228	1 1 1 0 0 1 0 0	E4	73	140	1 0 0 0 1 1 0 0	8C
29	244	1 1 1 1 0 1 0 0	F4	74	158	1 0 0 1 1 1 1 0	9E
30	230	1 1 1 0 0 1 1 0	E6	75	142	1 0 0 0 1 1 1 0	8E
31	246	1 1 1 1 0 1 1 0	F6	76	148	1 0 0 1 0 1 0 0	94
32	201	1 1 0 0 1 0 0 1	C9	77	132	1 0 0 0 0 1 0 0	84
33	217	1 1 0 1 1 0 0 1	D9	78	150	1 0 0 1 0 1 1 0	96
34	203	1 1 0 0 1 0 1 1	CB	79	134	1 0 0 0 0 1 1 0	86
35	219	1 1 0 1 1 0 1 1	DB	80	184	1 0 1 1 1 0 0 0	B8
36	193	1 1 0 0 0 0 0 1	C1	81	168	1 0 1 0 1 0 0 0	A8
37	209	1 1 0 1 0 0 0 1	D1	82	186	1 0 1 1 1 0 1 0	BA
38	195	1 1 0 0 0 0 1 1	C3	83	170	1 0 1 0 1 0 1 0	AA
39	211	1 1 0 1 0 0 1 1	D3	84	176	1 0 1 1 0 0 0 0	B0
40	205	1 1 0 0 1 1 0 1	CD	85	160	1 0 1 0 0 0 0 0	A0
41	221	1 1 0 1 1 1 0 1	DD	86	178	1 0 1 1 0 0 1 0	B2
42	207	1 1 0 0 1 1 1 1	CF	87	162	1 0 1 0 0 0 1 0	A2
43	223	1 1 0 1 1 1 1 1	DF	88	188	1 0 1 1 1 1 0 0	BC
44	197	1 1 0 0 0 1 0 1	C5	89	172	1 0 1 0 1 1 0 0	AC

Table 1 Continued

Internal Dec.	External Dec.	External Binary	External Hex
90	190	1 0 1 1 1 1 1 0	BE
91	174	1 0 1 0 1 1 1 0	AE
92	180	1 0 1 1 0 1 0 0	B4
93	164	1 0 1 0 0 1 0 0	A4
94	182	1 0 1 1 0 1 1 0	B6
95	166	1 0 1 0 0 1 1 0	A6
96	153	1 0 0 1 1 0 0 1	99
97	137	1 0 0 0 1 0 0 1	89
98	155	1 0 0 1 1 0 1 1	9B
99	139	1 0 0 0 1 0 1 1	8B
100	145	1 0 0 1 0 0 0 1	91
101	129	1 0 0 0 0 0 0 1	81
102	147	1 0 0 1 0 0 1 1	93
103	131	1 0 0 0 0 0 1 1	83
104	157	1 0 0 1 1 1 0 1	9D
105	141	1 0 0 0 1 1 0 1	8D
106	159	1 0 0 1 1 1 1 1	9F
107	143	1 0 0 0 1 1 1 1	8F
108	149	1 0 0 1 0 1 0 1	95
109	133	1 0 0 0 0 1 0 1	85
110	151	1 0 0 1 0 1 1 1	97
111	135	1 0 0 0 0 1 1 1	87
112	185	1 0 1 1 1 0 0 1	B9
113	169	1 0 1 0 1 0 0 1	A9
114	187	1 0 1 1 1 0 1 1	BB
115	171	1 0 1 0 1 0 1 1	AB
116	177	1 0 1 1 0 0 0 1	B1
117	161	1 0 1 0 0 0 0 1	A1
118	179	1 0 1 1 0 0 1 1	B3
119	163	1 0 1 0 0 0 1 1	A3
120	189	1 0 1 1 1 1 0 1	BD
121	173	1 0 1 0 1 1 0 1	AD
122	191	1 0 1 1 1 1 1 1	BF
123	175	1 0 1 0 1 1 1 1	AF
124	181	1 0 1 1 0 1 0 1	B5
125	165	1 0 1 0 0 1 0 1	A5
126	183	1 0 1 1 0 1 1 1	B7
127	167	1 0 1 0 0 1 1 1	A7
128	39	0 0 1 0 0 1 1 1	27
129	55	0 0 1 1 0 1 1 1	37
130	37	0 0 1 0 0 1 0 1	25
131	53	0 0 1 1 0 1 0 1	35
132	47	0 0 1 0 1 1 1 1	2F
133	63	0 0 1 1 1 1 1 1	3F
134	45	0 0 1 0 1 1 0 1	2D
135	61	0 0 1 1 1 1 0 1	3D
136	35	0 0 1 0 0 0 1 1	23
137	51	0 0 1 1 0 0 1 1	33
138	33	0 0 1 0 0 0 0 1	21
139	49	0 0 1 1 0 0 0 1	31
140	43	0 0 1 0 1 0 1 1	2B
141	59	0 0 1 1 1 0 1 1	3B
142	41	0 0 1 0 1 0 0 1	29
143	57	0 0 1 1 1 0 0 1	39
144	7	0 0 0 0 0 1 1 1	07
145	23	0 0 0 1 0 1 1 1	17
146	5	0 0 0 0 0 1 0 1	05
147	21	0 0 0 1 0 1 0 1	15
148	15	0 0 0 0 1 1 1 1	0F
149	31	0 0 0 1 1 1 1 1	1F
150	13	0 0 0 0 1 1 0 1	0D
151	29	0 0 0 1 1 1 0 1	1D
152	3	0 0 0 0 0 0 1 1	03
153	19	0 0 0 1 0 0 1 1	13
154	1	0 0 0 0 0 0 0 1	01
155	17	0 0 0 1 0 0 0 1	11
156	11	0 0 0 0 1 0 1 1	0B
157	27	0 0 0 1 1 0 1 1	1B
158	9	0 0 0 0 1 0 0 1	09
159	25	0 0 0 1 1 0 0 1	19
160	38	0 0 1 0 0 1 1 0	26
161	54	0 0 1 1 0 1 1 0	36
162	36	0 0 1 0 0 1 0 0	24
163	52	0 0 1 1 0 1 0 0	34
164	46	0 0 1 0 1 1 1 0	2E
165	62	0 0 1 1 1 1 1 0	3E
166	44	0 0 1 0 1 1 0 0	2C
167	60	0 0 1 1 1 1 0 0	3C
168	34	0 0 1 0 0 0 1 0	22
169	50	0 0 1 1 0 0 1 0	32
170	32	0 0 1 0 0 0 0 0	20
171	48	0 0 1 1 0 0 0 0	30
172	42	0 0 1 0 1 0 1 0	2A
173	58	0 0 1 1 1 0 1 0	3A
174	40	0 0 1 0 1 0 0 0	28
175	56	0 0 1 1 1 0 0 0	38
176	6	0 0 0 0 0 1 1 0	06
177	22	0 0 0 1 0 1 1 0	16
178	4	0 0 0 0 0 1 0 0	04
179	20	0 0 0 1 0 1 0 0	14

III

Internal Dec.	External Dec.	External Binary	External Hex
180	14	0 0 0 0 1 1 1 0	0E
181	30	0 0 0 1 1 1 1 0	1E
182	12	0 0 0 0 1 1 0 0	0C
183	28	0 0 0 1 1 1 0 0	1C
184	2	0 0 0 0 0 0 1 0	02
185	18	0 0 0 1 0 0 1 0	12
186	0	0 0 0 0 0 0 0 0	00
187	16	0 0 0 1 0 0 0 0	10
188	10	0 0 0 0 1 0 1 0	0A
189	26	0 0 0 1 1 0 1 0	1A
190	8	0 0 0 0 1 0 0 0	08
191	24	0 0 0 1 1 0 0 0	18
192	119	0 1 1 1 0 1 1 1	77
193	103	0 1 1 0 0 1 1 1	67
194	117	0 1 1 1 0 1 0 1	75
195	101	0 1 1 0 0 1 0 1	65
196	127	0 1 1 1 1 1 1 1	7F
197	111	0 1 1 0 1 1 1 1	6F
198	125	0 1 1 1 1 1 0 1	7D
199	109	0 1 1 0 1 1 0 1	6D
200	115	0 1 1 1 0 0 1 1	73
201	99	0 1 1 0 0 0 1 1	63
202	113	0 1 1 1 0 0 0 1	71
203	97	0 1 1 0 0 0 0 1	61
204	123	0 1 1 1 1 0 1 1	7B
205	107	0 1 1 0 1 0 1 1	6B
206	121	0 1 1 1 1 0 0 1	79
207	105	0 1 1 0 1 0 0 1	69
208	87	0 1 0 1 0 1 1 1	57
209	71	0 1 0 0 0 1 1 1	47
210	85	0 1 0 1 0 1 0 1	55
211	69	0 1 0 0 0 1 0 1	45
212	95	0 1 0 1 1 1 1 1	5F
213	79	0 1 0 0 1 1 1 1	4F
214	93	0 1 0 1 1 1 0 1	5D
215	77	0 1 0 0 1 1 0 1	4D
216	83	0 1 0 1 0 0 1 1	53
217	67	0 1 0 0 0 0 1 1	43
218	81	0 1 0 1 0 0 0 1	51
219	65	0 1 0 0 0 0 0 1	41
220	91	0 1 0 1 1 0 1 1	5B
221	75	0 1 0 0 1 0 1 1	4B
222	89	0 1 0 1 1 0 0 1	59
223	73	0 1 0 0 1 0 0 1	49
224	118	0 1 1 1 0 1 1 0	76
225	102	0 1 1 0 0 1 1 0	66
226	116	0 1 1 1 0 1 0 0	74
227	100	0 1 1 0 0 1 0 0	64
228	126	0 1 1 1 1 1 1 0	7E
229	110	0 1 1 0 1 1 1 0	6E
230	124	0 1 1 1 1 1 0 0	7C
231	108	0 1 1 0 1 1 0 0	6C
232	114	0 1 1 1 0 0 1 0	72
233	98	0 1 1 0 0 0 1 0	62
234	112	0 1 1 1 0 0 0 0	70
235	96	0 1 1 0 0 0 0 0	60
236	122	0 1 1 1 1 0 1 0	7A
237	106	0 1 1 0 1 0 1 0	6A
238	120	0 1 1 1 1 0 0 0	78
239	104	0 1 1 0 1 0 0 0	68
240	86	0 1 0 1 0 1 1 0	56
241	70	0 1 0 0 0 1 1 0	46
242	84	0 1 0 1 0 1 0 0	54
243	68	0 1 0 0 0 1 0 0	44
244	94	0 1 0 1 1 1 1 0	5E
245	78	0 1 0 0 1 1 1 0	4E
246	92	0 1 0 1 1 1 0 0	5C
247	76	0 1 0 0 1 1 0 0	4C
248	82	0 1 0 1 0 0 1 0	52
249	66	0 1 0 0 0 0 1 0	42
250	80	0 1 0 1 0 0 0 0	50
251	64	0 1 0 0 0 0 0 0	40
252	90	0 1 0 1 1 0 1 0	5A
253	74	0 1 0 0 1 0 1 0	4A
254	88	0 1 0 1 1 0 0 0	58
255	72	0 1 0 0 1 0 0 0	48

MK4564 TOPOGRAPHICAL MAP COLUMN ADDRESS RELATIONSHIPS

Table 2

Internal Dec.	External Dec.	External Binary	External Hex
0	0	0 0 0 0 0 0 0 0	00
1	16	0 0 0 1 0 0 0 0	10
2	128	1 0 0 0 0 0 0 0	80
3	144	1 0 0 1 0 0 0 0	90
4	4	0 0 0 0 0 1 0 0	04
5	20	0 0 0 1 0 1 0 0	14
6	132	1 0 0 0 0 1 0 0	84
7	148	1 0 0 1 0 1 0 0	94
8	32	0 0 1 0 0 0 0 0	20
9	48	0 0 1 1 0 0 0 0	30
10	160	1 0 1 0 0 0 0 0	A0
11	176	1 0 1 1 0 0 0 0	B0
12	36	0 0 1 0 0 1 0 0	24
13	52	0 0 1 1 0 1 0 0	34
14	164	1 0 1 0 0 1 0 0	A4
15	180	1 0 1 1 0 1 0 0	B4
16	1	0 0 0 0 0 0 0 1	01
17	17	0 0 0 1 0 0 0 1	11
18	129	1 0 0 0 0 0 0 1	81
19	145	1 0 0 1 0 0 0 1	91
20	5	0 0 0 0 0 1 0 1	05
21	21	0 0 0 1 0 1 0 1	15
22	133	1 0 0 0 0 1 0 1	85
23	149	1 0 0 1 0 1 0 1	95
24	33	0 0 1 0 0 0 0 1	21
25	49	0 0 1 1 0 0 0 1	31
26	161	1 0 1 0 0 0 0 1	A1
27	177	1 0 1 1 0 0 0 1	B1
28	37	0 0 1 0 0 1 0 1	25
29	53	0 0 1 1 0 1 0 1	35
30	165	1 0 1 0 0 1 0 1	A5
31	181	1 0 1 1 0 1 0 1	B5
32	2	0 0 0 0 0 0 1 0	02
33	18	0 0 0 1 0 0 1 0	12
34	130	1 0 0 0 0 0 1 0	82
35	146	1 0 0 1 0 0 1 0	92
36	6	0 0 0 0 0 1 1 0	06
37	22	0 0 0 1 0 1 1 0	16
38	134	1 0 0 0 0 1 1 0	86
39	150	1 0 0 1 0 1 1 0	96
40	34	0 0 1 0 0 0 1 0	22
41	50	0 0 1 1 0 0 1 0	32
42	162	1 0 1 0 0 0 1 0	A2
43	178	1 0 1 1 0 0 1 0	B2
44	38	0 0 1 0 0 1 1 0	26
45	54	0 0 1 1 0 1 1 0	36
46	166	1 0 1 0 0 1 1 0	A6
47	182	1 0 1 1 0 1 1 0	B6
48	3	0 0 0 0 0 0 1 1	03
49	19	0 0 0 1 0 0 1 1	13
50	131	1 0 0 0 0 0 1 1	83
51	147	1 0 0 1 0 0 1 1	93
52	7	0 0 0 0 0 1 1 1	07
53	23	0 0 0 1 0 1 1 1	17
54	135	1 0 0 0 0 1 1 1	87
55	151	1 0 0 1 0 1 1 1	97
56	35	0 0 1 0 0 0 1 1	23
57	51	0 0 1 1 0 0 1 1	33
58	163	1 0 1 0 0 0 1 1	A3
59	179	1 0 1 1 0 0 1 1	B3
60	39	0 0 1 0 0 1 1 1	27
61	55	0 0 1 1 0 1 1 1	37
62	167	1 0 1 0 0 1 1 1	A7
63	183	1 0 1 1 0 1 1 1	B7
64	8	0 0 0 0 1 0 0 0	08
65	24	0 0 0 1 1 0 0 0	18
66	136	1 0 0 0 1 0 0 0	88
67	152	1 0 0 1 1 0 0 0	98
68	12	0 0 0 0 1 1 0 0	0C
69	28	0 0 0 1 1 1 0 0	1C
70	140	1 0 0 0 1 1 0 0	8C
71	156	1 0 0 1 1 1 0 0	9C
72	40	0 0 1 0 1 0 0 0	28
73	56	0 0 1 1 1 0 0 0	38
74	168	1 0 1 0 1 0 0 0	A8
75	184	1 0 1 1 1 0 0 0	B8
76	44	0 0 1 0 1 1 0 0	2C
77	60	0 0 1 1 1 1 0 0	3C
78	172	1 0 1 0 1 1 0 0	AC
79	188	1 0 1 1 1 1 0 0	BC
80	9	0 0 0 0 1 0 0 1	09
81	25	0 0 0 1 1 0 0 1	19
82	137	1 0 0 0 1 0 0 1	89
83	153	1 0 0 1 1 0 0 1	99
84	13	0 0 0 0 1 1 0 1	0D
85	29	0 0 0 1 1 1 0 1	1D
86	141	1 0 0 0 1 1 0 1	8D
87	157	1 0 0 1 1 1 0 1	9D
88	41	0 0 1 0 1 0 0 1	29
89	57	0 0 1 1 1 0 0 1	39

III

Table 2 (cont'd)

Internal Dec.	External Dec.	External Binary	External Hex
90	169	1 0 1 0 1 0 0 1	A9
91	185	1 0 1 1 1 0 0 1	B9
92	45	0 0 1 0 1 1 0 1	2D
93	61	0 0 1 1 1 1 0 1	3D
94	173	1 0 1 0 1 1 0 1	AD
95	189	1 0 1 1 1 1 0 1	BD
96	10	0 0 0 0 1 0 1 0	0A
97	26	0 0 0 1 1 0 1 0	1A
98	138	1 0 0 0 1 0 1 0	8A
99	154	1 0 0 1 1 0 1 0	9A
100	14	0 0 0 0 1 1 1 0	0E
101	30	0 0 0 1 1 1 1 0	1E
102	142	1 0 0 0 1 1 1 0	8E
103	158	1 0 0 1 1 1 1 0	9E
104	42	0 0 1 0 1 0 1 0	2A
105	58	0 0 1 1 1 0 1 0	3A
106	170	1 0 1 0 1 0 1 0	AA
107	186	1 0 1 1 1 0 1 0	BA
108	46	0 0 1 0 1 1 1 0	2E
109	62	0 0 1 1 1 1 1 0	3E
110	174	1 0 1 0 1 1 1 0	AE
111	190	1 0 1 1 1 1 1 0	BE
112	11	0 0 0 0 1 0 1 1	0B
113	27	0 0 0 1 1 0 1 1	1B
114	139	1 0 0 0 1 0 1 1	8B
115	155	1 0 0 1 1 0 1 1	9B
116	15	0 0 0 0 1 1 1 1	0F
117	31	0 0 0 1 1 1 1 1	1F
118	143	1 0 0 0 1 1 1 1	8F
119	159	1 0 0 1 1 1 1 1	9F
120	43	0 0 1 0 1 0 1 1	2B
121	59	0 0 1 1 1 0 1 1	3B
122	171	1 0 1 0 1 0 1 1	AB
123	187	1 0 1 1 1 0 1 1	BB
124	47	0 0 1 0 1 1 1 1	2F
125	63	0 0 1 1 1 1 1 1	3F
126	175	1 0 1 0 1 1 1 1	AF
127	191	1 0 1 1 1 1 1 1	BF
128	64	0 1 0 0 0 0 0 0	40
129	80	0 1 0 1 0 0 0 0	50
130	192	1 1 0 0 0 0 0 0	C0
131	208	1 1 0 1 0 0 0 0	D0
132	68	0 1 0 0 0 1 0 0	44
133	84	0 1 0 1 0 1 0 0	54
134	196	1 1 0 0 0 1 0 0	C4
135	212	1 1 0 1 0 1 0 0	D4
136	96	0 1 1 0 0 0 0 0	60
137	112	0 1 1 1 0 0 0 0	70
138	224	1 1 1 0 0 0 0 0	E0
139	240	1 1 1 1 0 0 0 0	F0
140	100	0 1 1 0 0 1 0 0	64
141	116	0 1 1 1 0 1 0 0	74
142	228	1 1 1 0 0 1 0 0	E4
143	244	1 1 1 1 0 1 0 0	F4
144	65	0 1 0 0 0 0 0 1	41
145	81	0 1 0 1 0 0 0 1	51
146	193	1 1 0 0 0 0 0 1	C1
147	209	1 1 0 1 0 0 0 1	D1
148	69	0 1 0 0 0 1 0 1	45
149	85	0 1 0 1 0 1 0 1	55
150	197	1 1 0 0 0 1 0 1	C5
151	213	1 1 0 1 0 1 0 1	D5
152	97	0 1 1 0 0 0 0 1	61
153	113	0 1 1 1 0 0 0 1	71
154	225	1 1 1 0 0 0 0 1	E1
155	241	1 1 1 1 0 0 0 1	F1
156	101	0 1 1 0 0 1 0 1	65
157	117	0 1 1 1 0 1 0 1	75
158	229	1 1 1 0 0 1 0 1	E5
159	245	1 1 1 1 0 1 0 1	F5
160	66	0 1 0 0 0 0 1 0	42
161	82	0 1 0 1 0 0 1 0	52
162	194	1 1 0 0 0 0 1 0	C2
163	210	1 1 0 1 0 0 1 0	D2
164	70	0 1 0 0 0 1 1 0	46
165	86	0 1 0 1 0 1 1 0	56
166	198	1 1 0 0 0 1 1 0	C6
167	214	1 1 0 1 0 1 1 0	D6
168	98	0 1 1 0 0 0 1 0	62
169	114	0 1 1 1 0 0 1 0	72
170	226	1 1 1 0 0 0 1 0	E2
171	242	1 1 1 1 0 0 1 0	F2
172	102	0 1 1 0 0 1 1 0	66
173	118	0 1 1 1 0 1 1 0	76
174	230	1 1 1 0 0 1 1 0	E6
175	246	1 1 1 1 0 1 1 0	F6
176	67	0 1 0 0 0 0 1 1	43
177	83	0 1 0 1 0 0 1 1	53
178	195	1 1 0 0 0 0 1 1	C3
179	211	1 1 0 1 0 0 1 1	D3

Table 2 (cont'd)

Internal Dec.	External Dec.	External Binary	External Hex
180	71	0 1 0 0 0 1 1 1	47
181	87	0 1 0 1 0 1 1 1	57
182	199	1 1 0 0 0 1 1 1	C7
183	215	1 1 0 1 0 1 1 1	D7
184	99	0 1 1 0 0 0 1 1	63
185	115	0 1 1 1 0 0 1 1	73
186	227	1 1 1 0 0 0 1 1	E3
187	243	1 1 1 1 0 0 1 1	F3
188	103	0 1 1 0 0 1 1 1	67
189	119	0 1 1 1 0 1 1 1	77
190	231	1 1 1 0 0 1 1 1	E7
191	247	1 1 1 1 0 1 1 1	F7
192	72	0 1 0 0 1 0 0 0	48
193	88	0 1 0 1 1 0 0 0	58
194	200	1 1 0 0 1 0 0 0	C8
195	216	1 1 0 1 1 0 0 0	D8
196	76	0 1 0 0 1 1 0 0	4C
197	92	0 1 0 1 1 1 0 0	5C
198	204	1 1 0 0 1 1 0 0	CC
199	220	1 1 0 1 1 1 0 0	DC
200	104	0 1 1 0 1 0 0 0	68
201	120	0 1 1 1 1 0 0 0	78
202	232	1 1 1 0 1 0 0 0	E8
203	248	1 1 1 1 1 0 0 0	F8
204	108	0 1 1 0 1 1 0 0	6C
205	124	0 1 1 1 1 1 0 0	7C
206	236	1 1 1 0 1 1 0 0	EC
207	252	1 1 1 1 1 1 0 0	FC
208	73	0 1 0 0 1 0 0 1	49
209	89	0 1 0 1 1 0 0 1	59
210	201	1 1 0 0 1 0 0 1	C9
211	217	1 1 0 1 1 0 0 1	D9
212	77	0 1 0 0 1 1 0 1	4D
213	93	0 1 0 1 1 1 0 1	5D
214	205	1 1 0 0 1 1 0 1	CD
215	221	1 1 0 1 1 1 0 1	DD
216	105	0 1 1 0 1 0 0 1	69
217	121	0 1 1 1 1 0 0 1	79
218	233	1 1 1 0 1 0 0 1	E9
219	249	1 1 1 1 1 0 0 1	F9
220	109	0 1 1 0 1 1 0 1	6D
221	125	0 1 1 1 1 1 0 1	7D
222	237	1 1 1 0 1 1 0 1	ED
223	253	1 1 1 1 1 1 0 1	FD
224	74	0 1 0 0 1 0 1 0	4A
225	90	0 1 0 1 1 0 1 0	5A
226	202	1 1 0 0 1 0 1 0	CA
227	218	1 1 0 1 1 0 1 0	DA
228	78	0 1 0 0 1 1 1 0	4E
229	94	0 1 0 1 1 1 1 0	5E
230	206	1 1 0 0 1 1 1 0	CE
231	222	1 1 0 1 1 1 1 0	DE
232	106	0 1 1 0 1 0 1 0	6A
233	122	0 1 1 1 1 0 1 0	7A
234	234	1 1 1 0 1 0 1 0	EA
235	250	1 1 1 1 1 0 1 0	FA
236	110	0 1 1 0 1 1 1 0	6E
237	126	0 1 1 1 1 1 1 0	7E
238	238	1 1 1 0 1 1 1 0	EE
239	254	1 1 1 1 1 1 1 0	FE
240	75	0 1 0 0 1 0 1 1	4B
241	91	0 1 0 1 1 0 1 1	5B
242	203	1 1 0 0 1 0 1 1	CB
243	219	1 1 0 1 1 0 1 1	DB
244	79	0 1 0 0 1 1 1 1	4F
245	95	0 1 0 1 1 1 1 1	5F
246	207	1 1 0 0 1 1 1 1	CF
247	223	1 1 0 1 1 1 1 1	DF
248	107	0 1 1 0 1 0 1 1	6B
249	123	0 1 1 1 1 0 1 1	7B
250	235	1 1 1 0 1 0 1 1	EB
251	251	1 1 1 1 1 0 1 1	FB
252	111	0 1 1 0 1 1 1 1	6F
253	127	0 1 1 1 1 1 1 1	7F
254	239	1 1 1 0 1 1 1 1	EF
255	255	1 1 1 1 1 1 1 1	FF

Z8000 MEMORY INTERFACING TECHNIQUES

Application Note

INTRODUCTION

The 16-bit microprocessor technology has brought large scale computing power to a single chip. This processing capability is only useful if all system components are equally powerful. The expense, space and power requirements of memory expansion have been a major factor in the limitations of computer systems to date. The introduction of the MK4564, new generation 64K dynamic RAM, should alleviate these memory problems.

FUNCTIONAL DESCRIPTION

The MK4564 is organized as 65,536 words by 1 bit. Memory locations are accessed by the now industry standard multiplexed address technique pioneered by Mostek. The proper cell is selected by first latching the 8 row address bits with a high-to-low transition on the row address strobe, $\overline{RAS}$, pin followed by latching the 8 column address bits with a high-to-low transition on the column address strobe, $\overline{CAS}$, pin. $\overline{RAS}$, derived from the processor's $\overline{MREQ}$ signal, activates the high, the low or both bytes of memory. Column address bits are selected on the next clock edge, ensuring $\overline{RAS}$ propagation through all gate delays in preparation of $\overline{CAS}$ which is generated from the processor's $\overline{DS}$ signal (see Figure 1, Z8001 to MK4564 Memory Interface and Figure 2, Z8000 Dynamic Memory Timing).

TECHNOLOGY BENEFITS

The MK4564 64K dynamic RAM reduces power consumption while quadrupling the memory capacity of its predecessor, the MK4116 16K RAM, maintaining the same package size. Previous generation memories required three power supplies. The MK4564 utilizes a single +5 V supply, thus simplifying board layout.

REFRESH

Refresh of the dynamic cell matrix in the MK4564 is accomplished by performing a memory cycle at each of the 128 row addresses within every 2 msec. interval. Although any normal memory cycle will perform the required refreshing, this function is most easily accomplished with "RAS-only" cycles. The RAS-only refresh cycle requires that a 7 bit refresh address (A0-A6) be valid at the device address inputs when RAS is asserted low.

The memory interface circuitry takes advantage of the Z8000's programmable on-chip counter to determine when the memory refresh should take place. Status bits ST0-ST3 are decoded for a refresh signal. This signal together with $\overline{MREQ}$ forms the $\overline{RAS}$ signal applied to all dynamic RAMs refreshing all of the memory array (see Figure 1, Z8001 to MK4564 Memory Interface and Figure 2, Refresh Timing).

MEMORY EXPANSION

The amount of memory can be expanded up to 8 megabytes by simply directing the $\overline{RAS}$ signal to the proper block of memory. This is accomplished by routing the $\overline{RAS}$ signal through a demultiplexer to the selected block, decoding segment numbers, SN1-SN6, which have already been latched. This technique allows all but the selected blocks to operate in the standby, low power, state. Care should be taken so that no more than the maximum number of memory devices be controlled by each TTL driver.

ROM INTERFACE

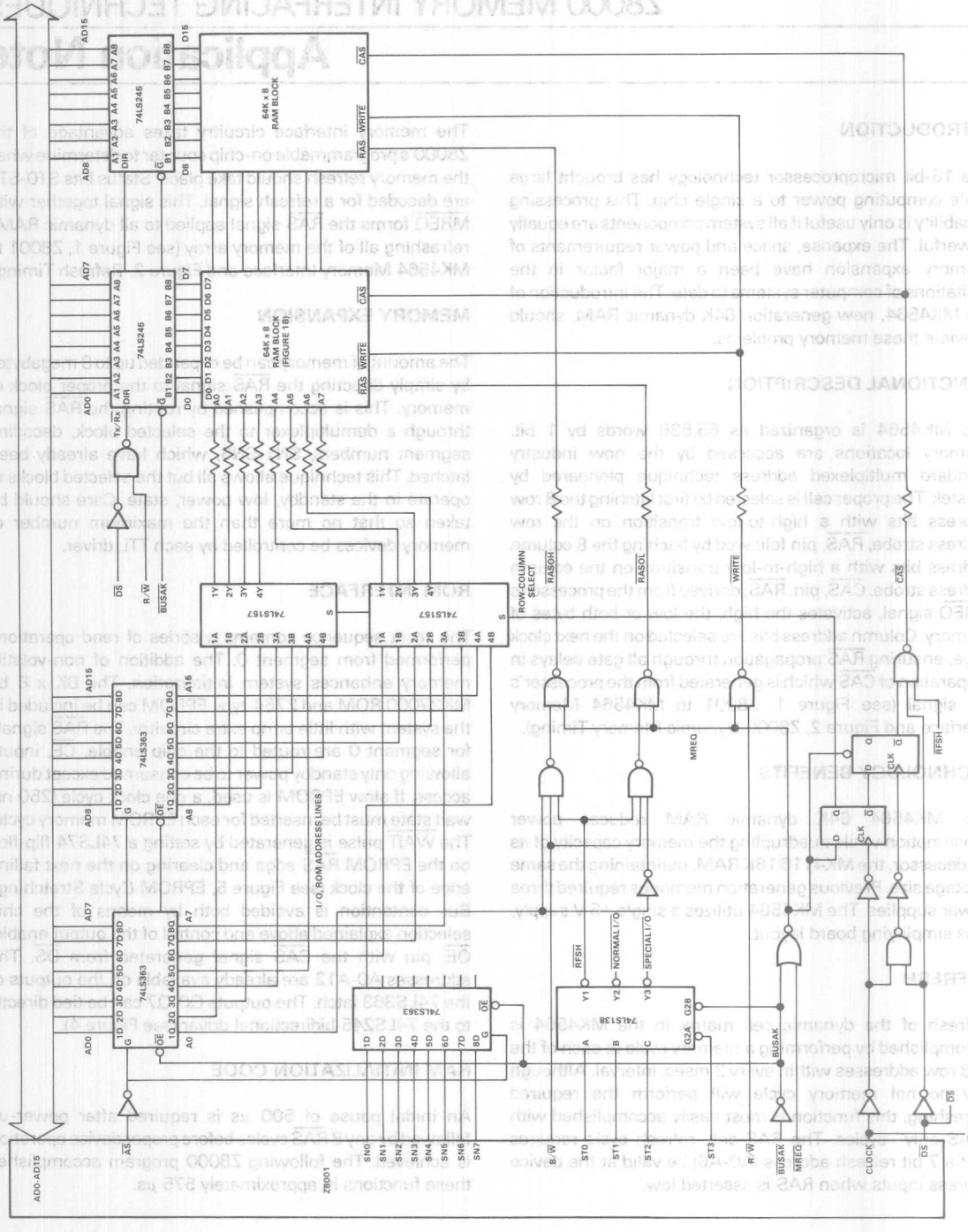
The reset sequence contains a series of read operations performed from segment 0. The addition of non-volatile memory enhances system initialization. The 8K x 8 bit MK37000 ROM and 2764-type EPROM can be included in the system with little or no extra circuitry. The $\overline{RAS}$ signals for segment 0 are routed to the chip enable, $\overline{CE}$, inputs allowing only standby power to be consumed except during access. If slow EPROM is used, a one clock cycle (250 ns) wait state must be inserted for each EPROM memory cycle. The $\overline{WAIT}$ pulse is generated by setting a 74LS74 flip-flop on the EPROM $\overline{RAS}$ edge and clearing on the next falling edge of the clock (see Figure 5, EPROM Cycle Stretching). Bus contention is avoided both by means of the chip selection explained above and control of the output enable, $\overline{OE}$, pin with the $\overline{CAS}$ signal generated from $\overline{DS}$. The addresses A0-A12 are already available on the outputs of the 74LS363 latch. The outputs Q0-Q7 can be tied directly to the 74LS245 bidirectional driver (see Figure 4).

RAM INITIALIZATION CODE

An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. The following Z8000 program accomplishes these functions in approximately 575 μs.

Z8001 TO MK4564 MEMORY INTERFACE

Figure 1A

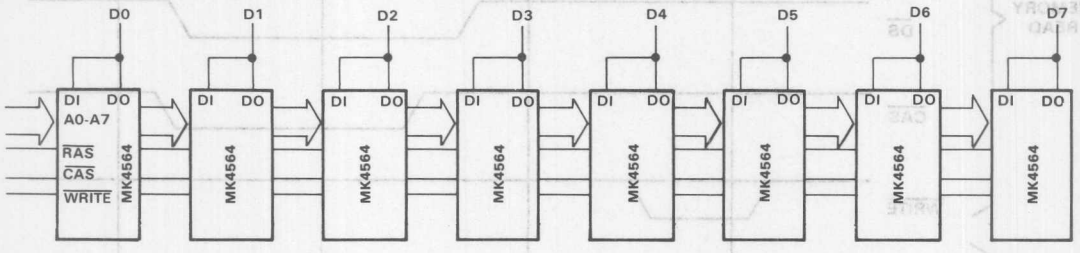


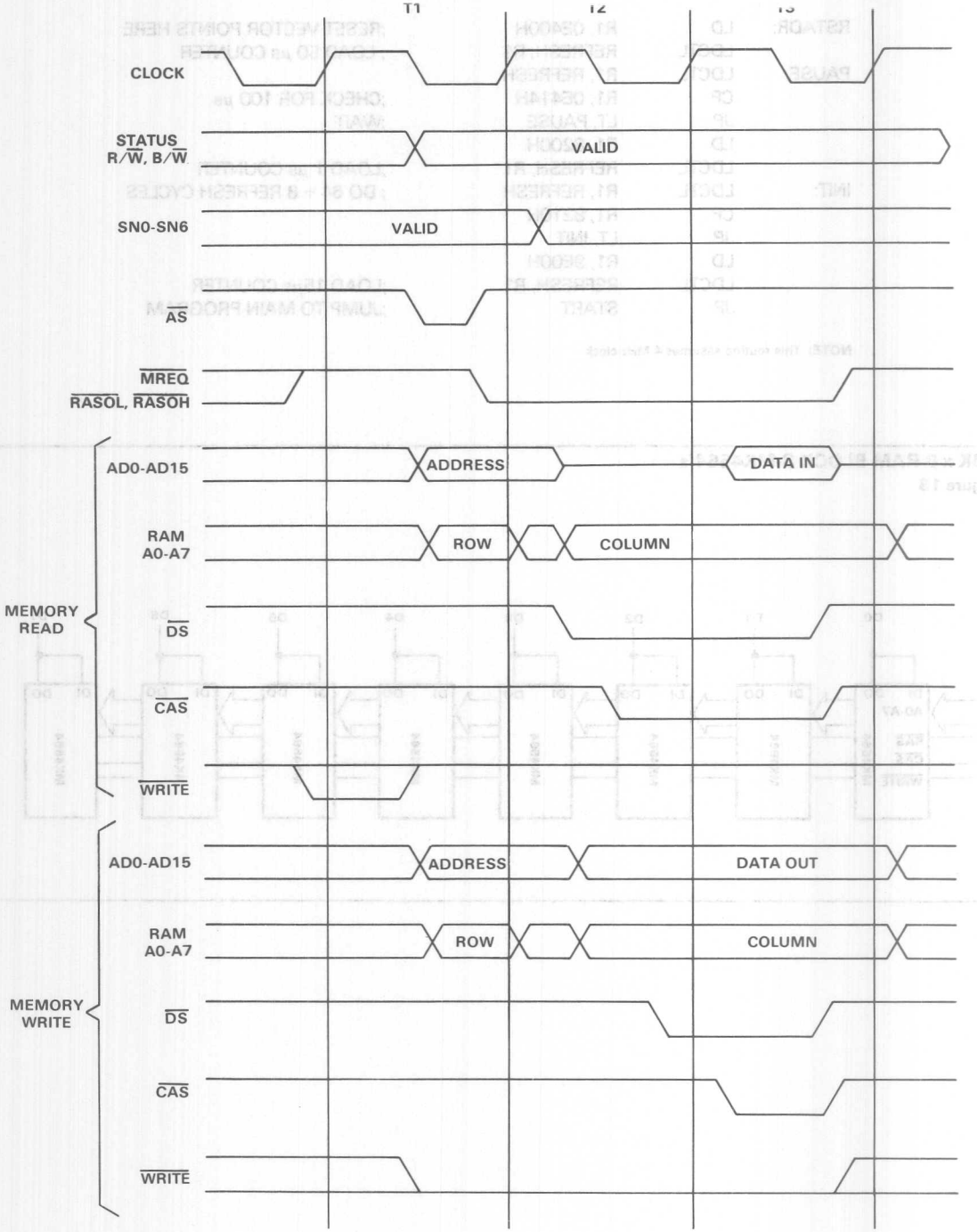
```
RSTADR:   LD       R1, 0E400H      ;RESET VECTOR POINTS HERE
          LDCTL    REFRESH, R1     ; LOAD 50 μs COUNTER
PAUSE:    LDCTL    R1, REFRESH
          CP       R1, 0E414H      ;CHECK FOR 100 μs
          JP       LT, PAUSE       ;WAIT
          LD       R1, 8200H
          LDCTL    REFRESH, R1     ;LOAD 1 μs COUNTER
INIT:     LDCTL    R1, REFRESH     ; DO 64 + 8 REFRESH CYCLES
          CP       R1, 8210H
          JP       LT, INIT
          LD       R1, 9E00H
          LDCTL    REFRESH, R1     ;LOAD 15μs COUNTER
          JP       START           ;JUMP TO MAIN PROGRAM
```

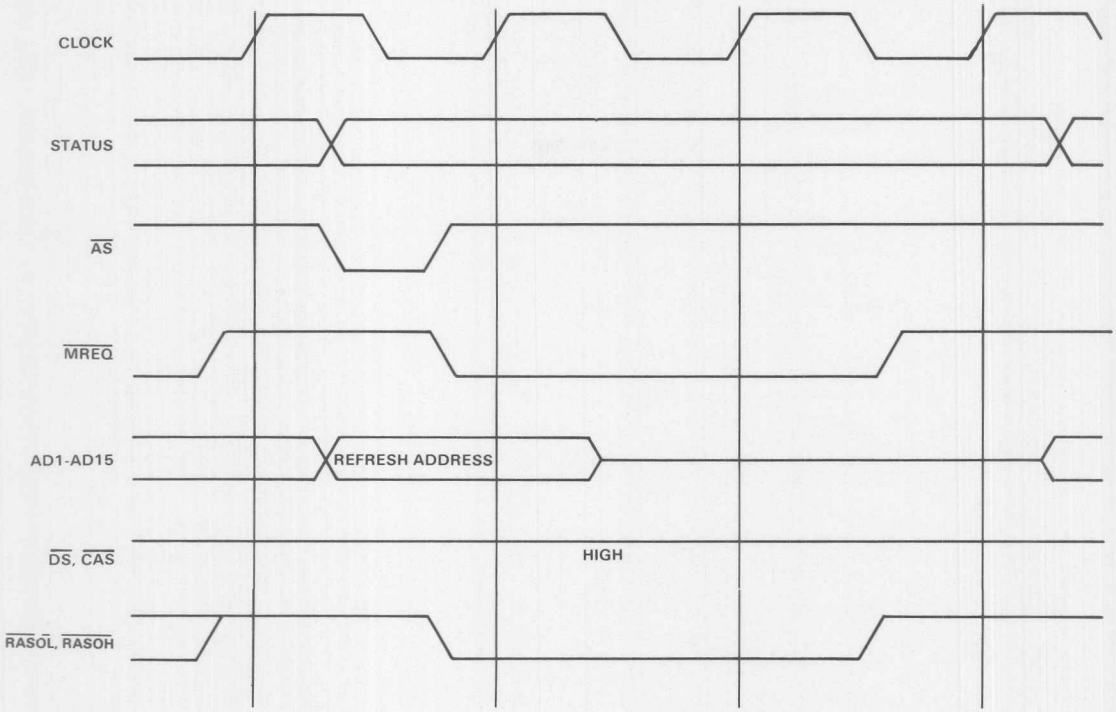
NOTE: This routine assumes 4 MHz clock

III

64K x 8 RAM BLOCK 8-MK4564's
Figure 1B



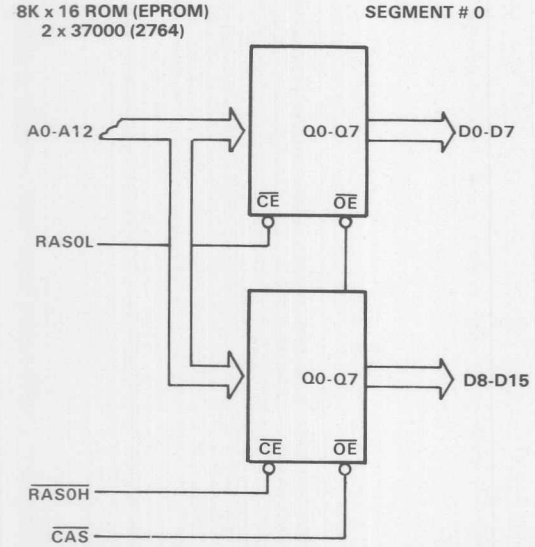

T1
T2
T3
CLOCK
STATUS
R/W, B/W
VALID
SN0-SN6
VALID
AS
MREQ
RASOL, RASOH
MEMORY READ
AD0-AD15
ADDRESS
DATA IN
RAM A0-A7
ROW
COLUMN
DS
CAS
WRITE
MEMORY WRITE
AD0-AD15
ADDRESS
DATA OUT
RAM A0-A7
ROW
COLUMN
DS
CAS
WRITE



III

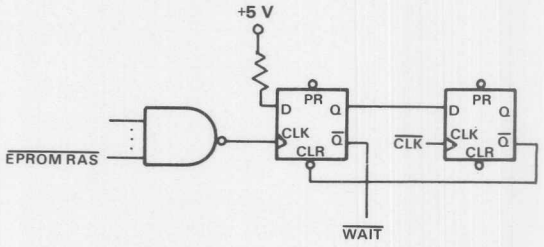
ROM MEMORY SEGMENT

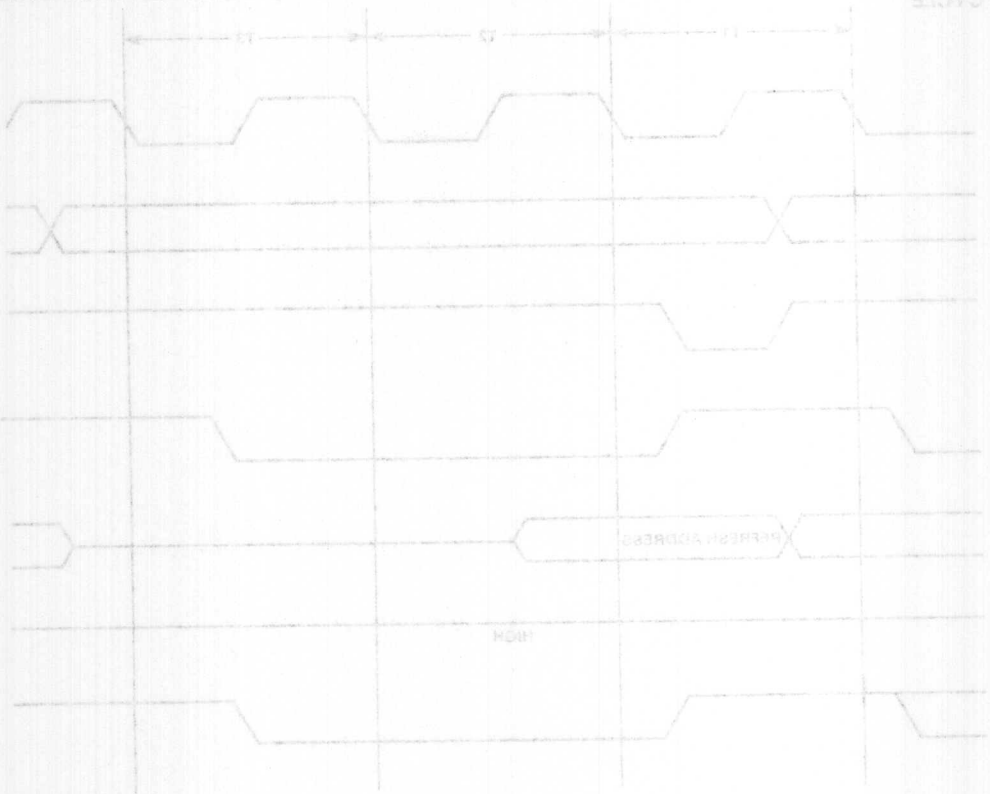
Figure 4

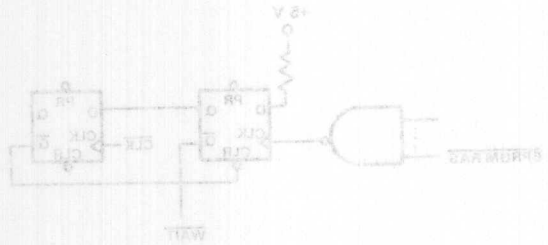


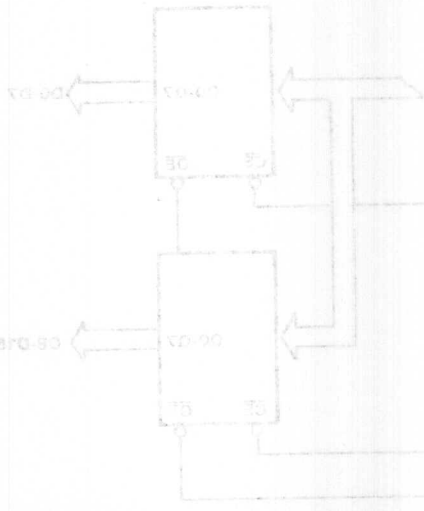
EPROM CYCLE STRETCHING

Figure 5









MOSTEK®

Z80 INTERFACING TECHNIQUES FOR DYNAMIC RAM

Application Note

INTRODUCTION

Since the introduction of second generation microprocessors, there has been a steady increase in the need for larger RAM memory for microcomputer systems. This need for larger RAM memory is due in part to the availability of higher level languages such as PL/M, PL/Z, FORTRAN, BASIC, and COBOL. Until now, when faced with the need to add memory to a microcomputer system, most designers have chosen static memories such as the 2102 1Kx1 or possibly one of the new 4Kx1 static memories. However, as most mini or mainframe memory designers have learned, 16-pin dynamic memories are often the best overall choice for reliability, low power, performance, and board density. This same philosophy is true for a microcomputer system. Why then have microcomputer designers been reluctant to use dynamic memory in their system? The most important reason is that second generation microprocessors such as the 8080 and 6800 do not provide the necessary signals to interface dynamic memories easily into a microcomputer system.

Today, with the introduction of the Z80, a true third generation microprocessor, not only can a microcomputer designer increase system throughput by the use of more powerful instructions, but he can also easily interface either static or dynamic memories into the microcomputer system. This application note provides specific examples of how to interface 16-pin dynamic memories to the Z80.

OPERATION OF 16-PIN DYNAMIC MEMORIES

The 16-pin dynamic memory concept, pioneered by MOSTEK, uses a unique address multiplexing technique which allows memories as large as 16, 384 bits x 1 to be packaged in a 16-pin package. For example the MK4027 (4,096x1 dynamic MOS RAM) and the MK4116 (16,384x1 dynamic MOS RAM) both use address multiplexing to load the address bits into memory. The MK4027 needs 12 address bits to select 1 out of 4,096 locations, while the MK4116 requires 14 bits to select 1 out of 16,384. The internal memories of the MK4027 and MK4116 can be thought of as a matrix. The MK4027 matrix can be thought of as 64x64, and the MK4116 as 128x128. To select a particular location, a row and column address is supplied to the memory. For the MK4027, address bits A_0-A_5 are the row address, and bits A_6-A_{11} are the column addresses. For the MK4116, address bits A_0-A_6 are the row address, and A_7-A_{13} are the column address. The row and column addresses are strobed into the memory by two negative going clocks called Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). By the use of $\overline{RAS}$ and $\overline{CAS}$, the address bits are latched into the memory for access to the desired memory location.

III

Dynamic memories store their data in the form of a charge on a small capacitor. In order for the dynamic memory to retain valid data, this charge must be periodically restored. The process by which data is restored in a dynamic memory is known as refreshing. A refresh cycle is performed on a row of data each time a read or write cycle is performed on any bit within the given row. A row consists of 64 locations for the MK4027 and 128 locations for the MK4116. The refresh period for the MK4027 and the MK4116 is 2ms which means that the memory will retain a row of data for 2ms without a refresh. Therefore, to refresh all rows within 2ms, a refresh cycle must be executed every 32μs (2ms÷64) for the MK4027, and 16μs (2ms÷ 128) for the MK4116.

To ensure that every row within a given memory is refreshed within the specified time, a refresh row address counter must be implemented either in external hardware or as an internal CPU function as in the Z80. (Discussed in more detail under Z80 Refresh Control and Timing.) The refresh row address counter should be incremented each time that a refresh cycle is executed. When a refresh is performed, all RAMs in the system should be loaded with the refresh row address. For the MK4027 and the MK4116, a refresh cycle consists of loading the refresh row address on the address lines and then generating a $\overline{RAS}$ for all RAMs in the system. This is known as a $\overline{RAS}$ only refresh. The row that was addressed will be refreshed in each memory. The $\overline{RAS}$ only refresh prevents a conflict between the outputs of all the RAMs by disabling the output on the MK4116, and maintaining the output state from the previous memory cycle on the MK4027.

Z80 TIMING AND MEMORY CONTROL SIGNALS

The Z80 was designed to make the job of interfacing

that are available to the designer. The Z80 control signals associated with memory operations are:

MEMORY REQUEST ($\overline{MREQ}$) - Memory request signal indicating that the address bus holds a valid memory address for a memory read, memory write, or memory refresh cycle.

READ ($\overline{RD}$) - Read signal indicating that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

WRITE ($\overline{WR}$) - Write signal indicating that the CPU data bus hold valid data to be stored in the addressed memory or I/O device.

REFRESH ($\overline{RFSH}$) - Refresh signal indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current MREQ signal should be used to generate a refresh cycle for all dynamic memories in the system.

Figures 1a, 1b, and 1c show the timing relationships of the control signals, address bus, data bus, and system clock Φ. By using these timing diagrams, a set of equations can be derived to show the worst case access times needed for dynamic memories with the Z80 operating at 2.5MHz.

The access time needed for the op code fetch cycle and the memory read cycle can be computed by equations 1 and 2.

(1) $t_{ACCESS\ OP\ CODE} = 3(t_c/2) - t_{DL\overline{\Phi}(MR)} - t_{S\Phi(D)}$

$t_{S\Phi(D)}$ = Data setup time to rising edge of clock during op code fetch cycle.

let: $t_C = 400ns$; $t_{DL\overline{\Phi}(MR)} = 100ns$; $t_{S\Phi} = 50ns$

then: $t_{ACCESS\ OP\ CODE} = 450ns$

(2) $t_{ACCESS\ MEMORY\ READ} = 4(t_c/2) - t_{DL\overline{\Phi}(MR)} - t_{S\overline{\Phi}(D)}$

where: t_C = Clock period

$t_{DL\overline{\Phi}(MR)}$ = $\overline{MREQ}$ delay from falling edge of clock

$t_{S\overline{\Phi}(D)}$ = Data Setup time to falling edge of clock

let: $t_C = 400ns$; $t_{DL\ (MR)} = 100ns$; $t_{S\ (D)\ \overline{\Phi}} = 60ns$

then: $t_{ACCESS\ MEMORY\ READ} = 640ns$

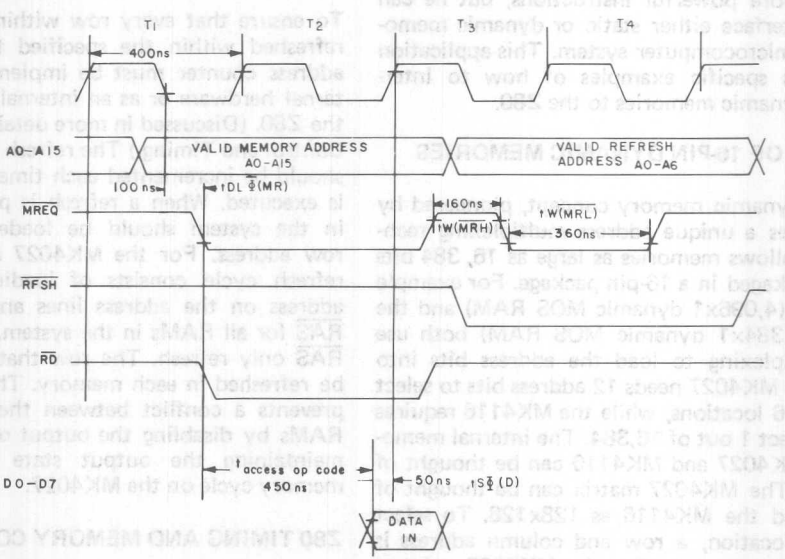
The access times computed in equations 1 and 2 are overall worst case access times required by the CPU. The overall access times must include all TTL buffer delays and the access time for the memory device. For example, a typical dynamic memory design would have the following characteristics (see Figure 2):

The example in Figure 2 shows an overall access time of 336ns. This would more than satisfy the 450ns required for the op code fetch and the 640ns required for a memory read.

CPU $\overline{MREQ}$ buffer delay	12ns (8T97)
Memory gating and timing delays	40ns
Memory device access time	250ns (MK4027/4116-4)
Memory data bus buffer delay	17ns (8T28)
CPU data bus buffer delay	17ns (8T28)
	336ns

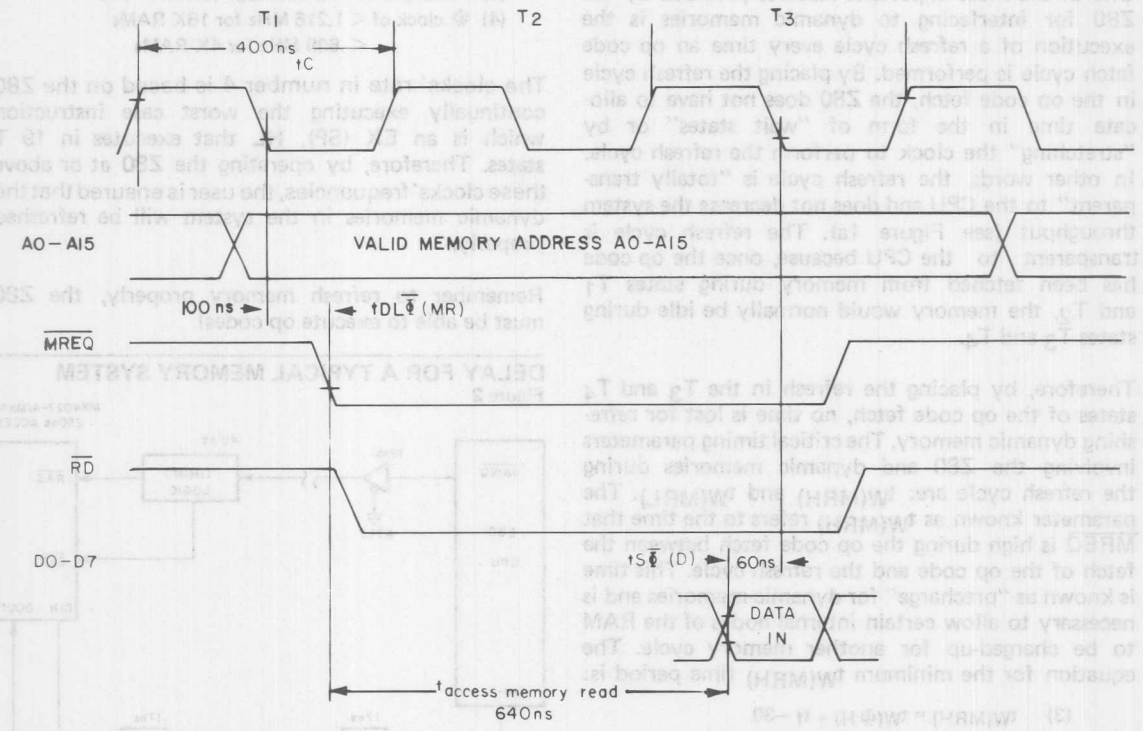
OP CODE FETCH TIMING

Figure 1a



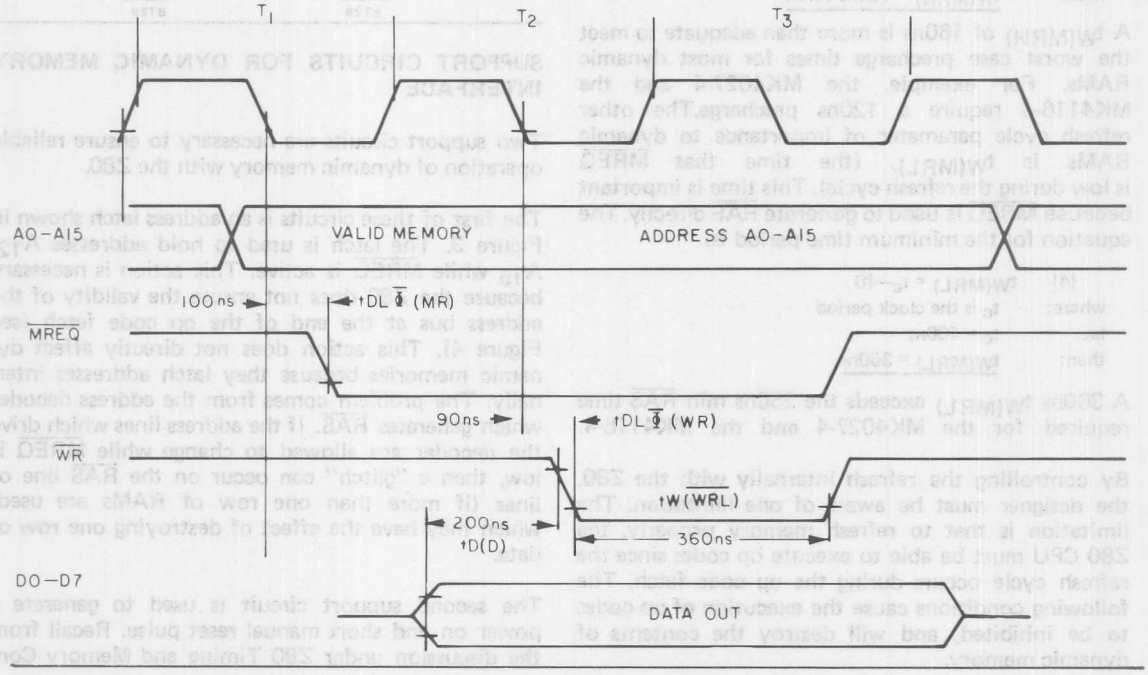
MEMORY READ TIMING

Figure 1b



MEMORY WRITE TIMING

Figure 1c



Z80 REFRESH CONTROL AND TIMING

One of the most important features provided by the Z80 for interfacing to dynamic memories is the execution of a refresh cycle every time an op code fetch cycle is performed. By placing the refresh cycle in the op code fetch, the Z80 does not have to allocate time in the form of "wait states" or by "stretching" the clock to perform the refresh cycle. In other words, the refresh cycle is "totally transparent" to the CPU and does not decrease the system throughput (see Figure 1a). The refresh cycle is transparent to the CPU because, once the op code has been fetched from memory during states T_1 and T_2, the memory would normally be idle during states T_3 and T_4.

Therefore, by placing the refresh in the T_3 and T_4 states of the op code fetch, no time is lost for refreshing dynamic memory. The critical timing parameters involving the Z80 and dynamic memories during the refresh cycle are: $t_{W(MRH)}$ and $t_{W(MRL)}$. The parameter known as $t_{W(MRH)}$ refers to the time that $\overline{MREQ}$ is high during the op code fetch between the fetch of the op code and the refresh cycle. This time is known as "precharge" for dynamic memories and is necessary to allow certain internal nodes of the RAM to be charged-up for another memory cycle. The equation for the minimum $t_{W(MRH)}$ time period is:

(3) $t_{W(MRH)} = t_{W(\Phi H)} + t_f - 30$

where: $t_{W(\Phi H)}$ is clock pulse width high
t_f is clock fall time

let: $t_{W(\Phi H)} = 180ns$; $t_f = 10ns$

then: $t_{W(MRH)} = 160ns$ (min)

A $t_{W(MRH)}$ of 160ns is more than adequate to meet the worst case precharge times for most dynamic RAMs. For example, the MK4027-4 and the MK4116-4 require a 120ns precharge.The other refresh cycle parameter of importance to dynamic RAMs is $t_{W(MRL)}$, (the time that $\overline{MREQ}$ is low during the refresh cycle). This time is important because $\overline{MREQ}$ is used to generate $\overline{RAS}$ directly. The equation for the minimum time period is:

(4) $t_{W(MRL)} = t_c - 40$

where: t_c is the clock period

let: $t_c = 400ns$

then: $t_{W(MRL)} = 360ns$

A 360ns $t_{W(MRL)}$ exceeds the 250ns min $\overline{RAS}$ time required for the MK4027-4 and the MK4116-4.

By controlling the refresh internally with the Z80, the designer must be aware of one limitation. The limitation is that to refresh memory properly, the Z80 CPU must be able to execute op codes since the refresh cycle occurs during the op code fetch. The following conditions cause the execution of op codes to be inhibited, and will destroy the contents of dynamic memory.

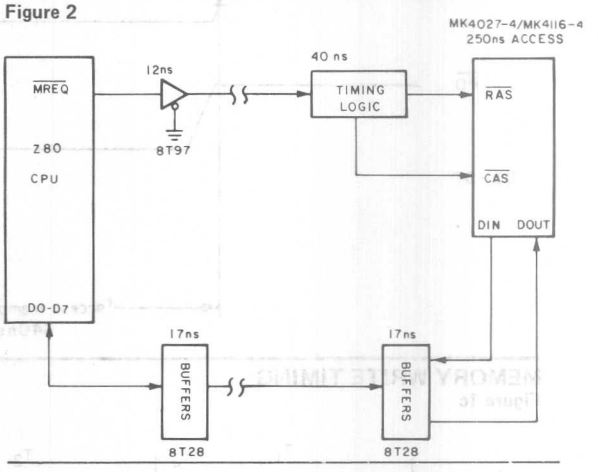
(1) Prolonged reset > 1ms
(2) Prolonged wait state operation > 1ms
(3) Prolonged bus acknowledge (DMA) > 1ms
(4) Φ clock of < 1.216 MHz for 16K RAMs
< .608 MHz for 4K RAMs

The clocks' rate in number 4 is based on the Z80 continually executing the worst case instruction which is an EX (SP), HL that executes in 19 T states. Therefore, by operating the Z80 at or above these clocks' frequencies, the user is ensured that the dynamic memories in the system will be refreshed properly.

Remember to refresh memory properly, the Z80 must be able to execute op codes!

DELAY FOR A TYPICAL MEMORY SYSTEM

Figure 2



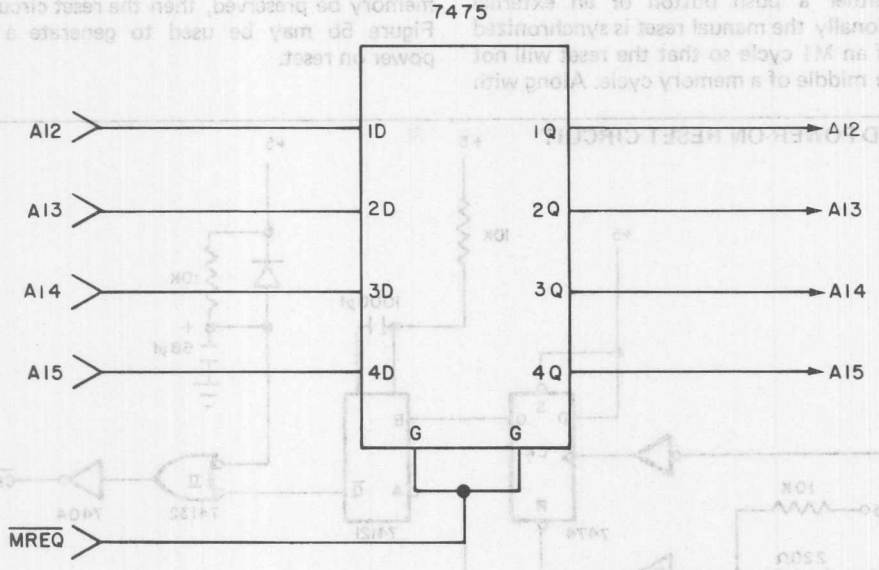
SUPPORT CIRCUITS FOR DYNAMIC MEMORY INTERFACE

Two support circuits are necessary to ensure reliable operation of dynamic memory with the Z80.

The first of these circuits is an address latch shown in Figure 3. The latch is used to hold addresses A_{12}-A_{15} while $\overline{MREQ}$ is active. This action is necessary because the Z80 does not ensure the validity of the address bus at the end of the op code fetch (see Figure 4). This action does not directly affect dynamic memories because they latch addresses internally. The problem comes from the address decoder which generates $\overline{RAS}$. If the address lines which drive the decoder are allowed to change while $\overline{MREQ}$ is low, then a "glitch" can occur on the $\overline{RAS}$ line or lines (if more than one row of RAMs are used) which may have the effect of destroying one row of data.

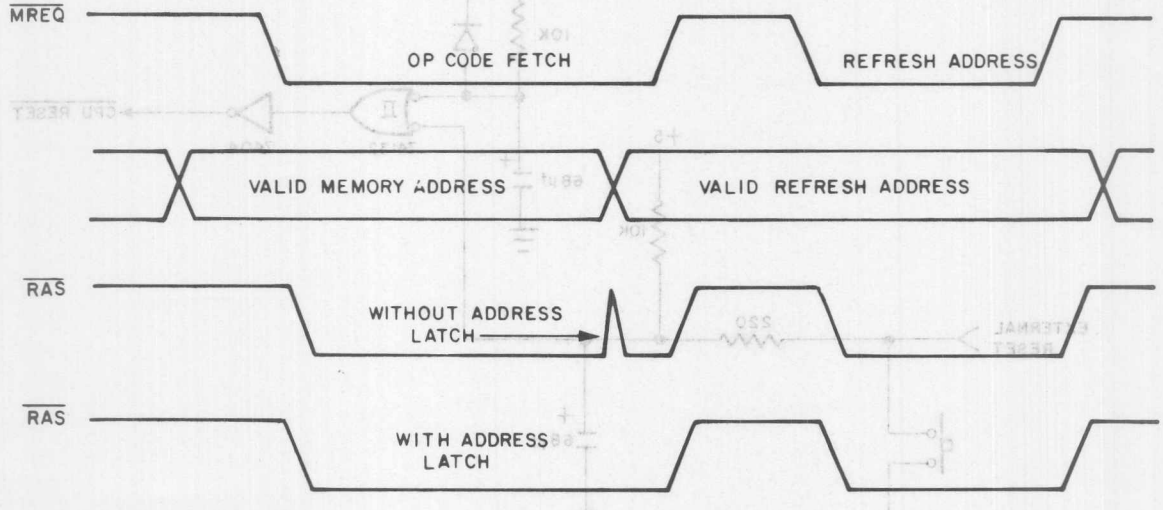
The second support circuit is used to generate a power on and short manual reset pulse. Recall from the discussion under Z80 Timing and Memory Con-

ADDRESS LATCH
Figure 3



III

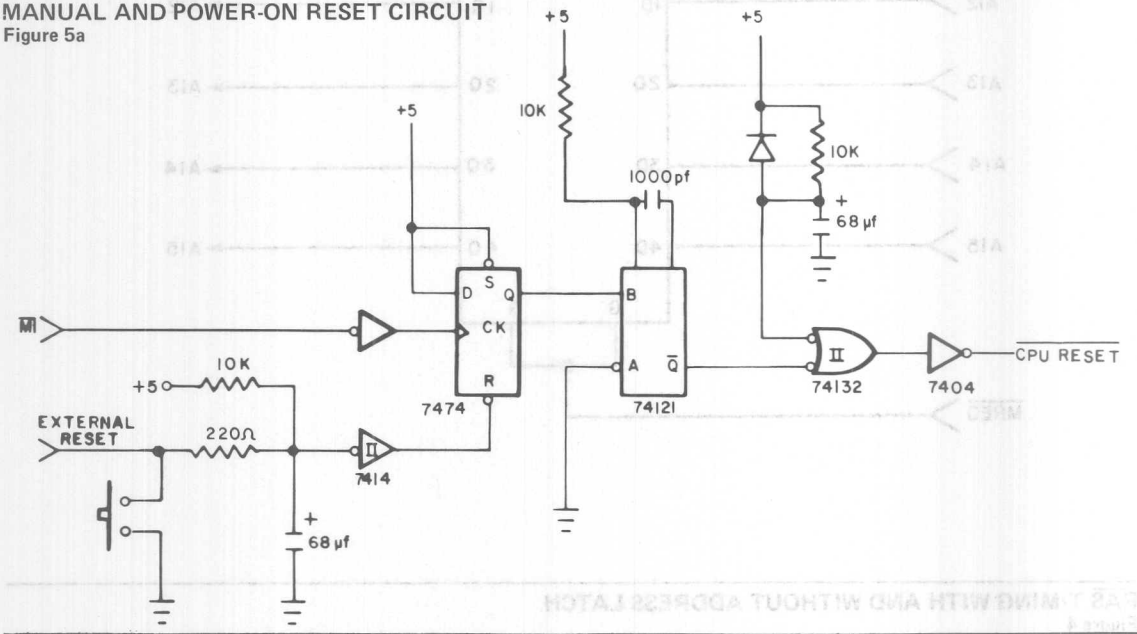
RAS TIMING WITH AND WITHOUT ADDRESS LATCH
Figure 4



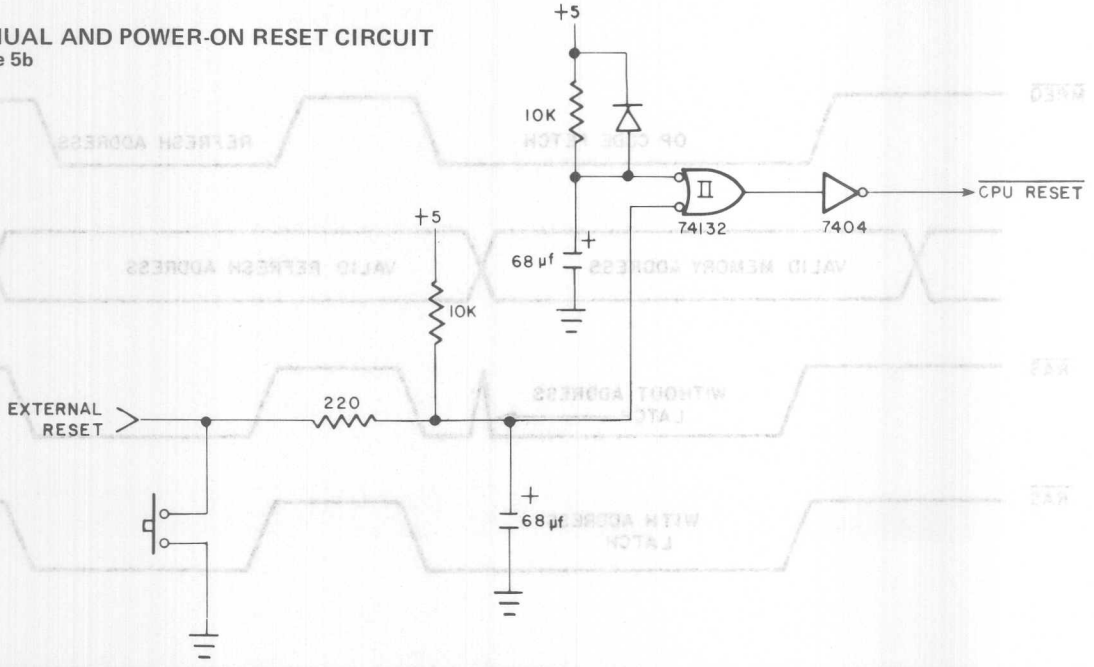
in Figure 5a can be used to generate a short reset pulse from either a push button or an external source. Additionally the manual reset is synchronized to the start of an M1 cycle so that the reset will not fall during the middle of a memory cycle. Along with

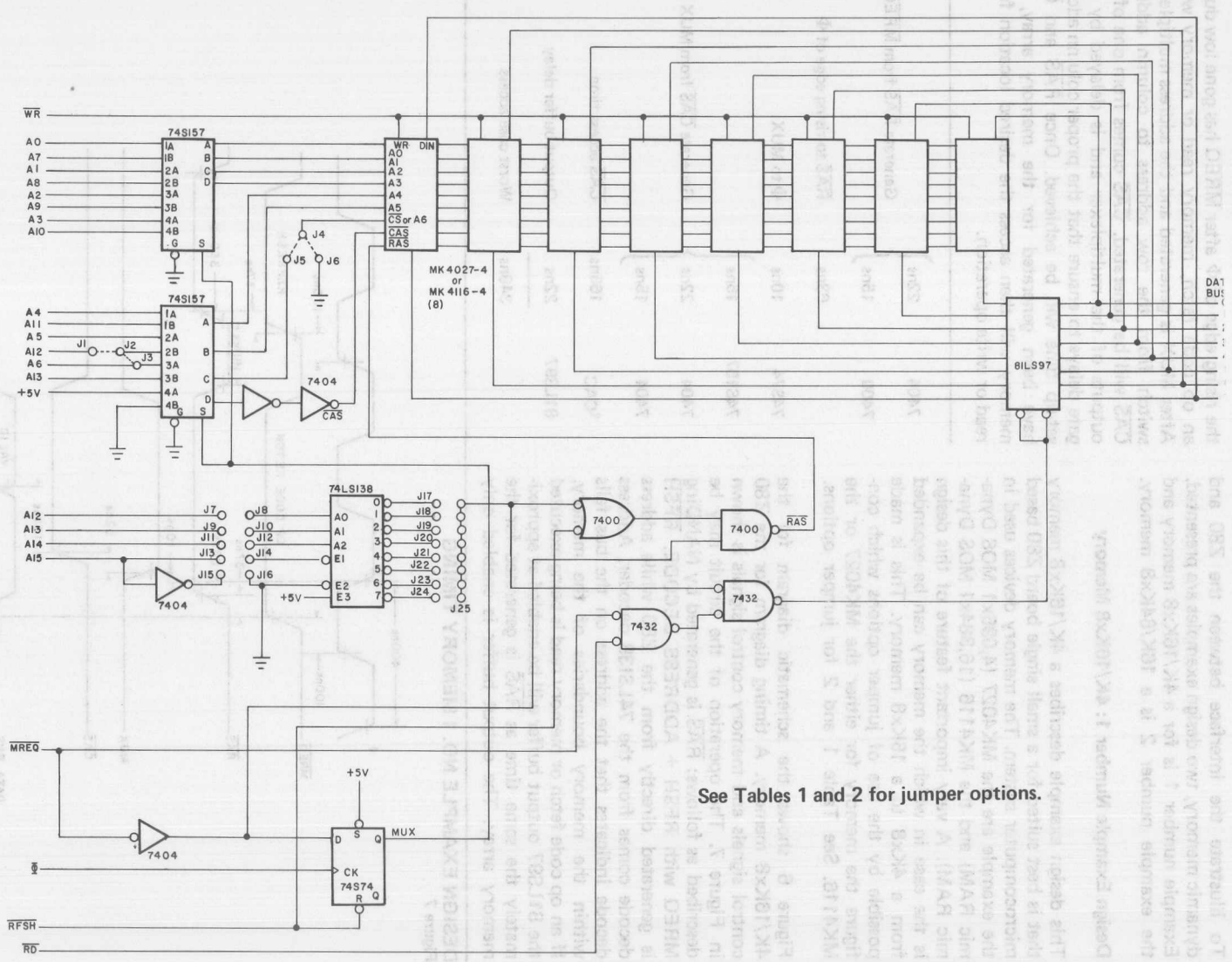
If it is not necessary that the contents of the dynamic memory be preserved, then the reset circuit shown in Figure 5b may be used to generate a manual or power on reset.

MANUAL AND POWER-ON RESET CIRCUIT
Figure 5a



MANUAL AND POWER-ON RESET CIRCUIT
Figure 5b





See Tables 1 and 2 for jumper options.

DESIGN EXAMPLES FOR INTERFACING THE Z80 TO DYNAMIC MEMORY

To illustrate the interface between the Z80 and dynamic memory, two design examples are presented. Example number 1 is for a 4K/16Kx8 memory and the example number 2 is a 16K/64Kx8 memory.

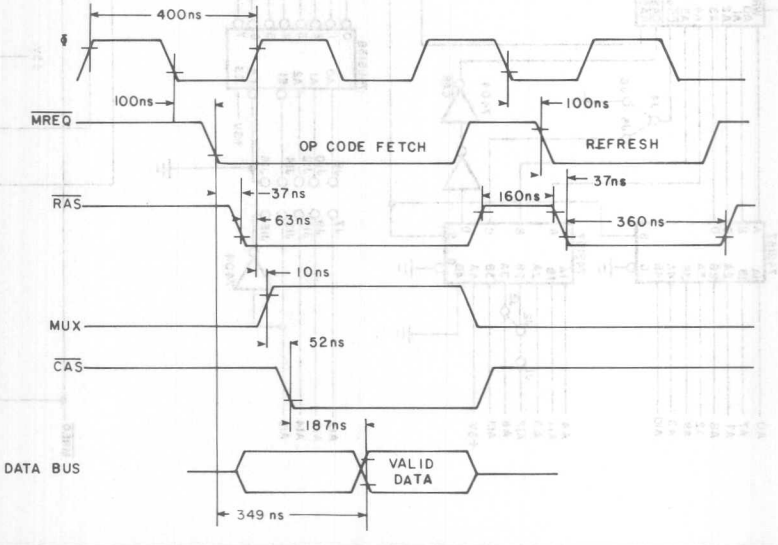
Design Example Number 1: 4K/16Kx8 Memory

This design example describes a 4K/16Kx8 memory that is best suited for a small single board Z80 based microcomputer system. The memory devices used in the example are the MK4027 (4,096x1 MOS Dynamic RAM) and the MK4116 (16,384x1 MOS Dynamic RAM). A very important feature of this design is the ease in which the memory can be expanded from a 4Kx8 to a 16Kx8 memory. This is made possible by the use of jumper options which configure the memory for either the MK4027 or the MK4116. See Table 1 and 2 for jumper options.

Figure 6 shows the schematic diagram for the 4K/16Kx8 memory. A timing diagram for the Z80 control signals and memory control signals is shown in Figure 7. The operation of the circuit may be described as follows: $\overline{RAS}$ is generated by NANDing MREQ with RFSH + ADDRESS DECODE. $\overline{RFSH}$ is generated directly from the Z80 while address decode comes from the 74LSI38 decoder. Address decode indicates that the address on the bus falls within the memory boundaries of the memory. If an op code fetch or memory read is being executed the 81LS97 output buffer will be enabled at approximately the same time as $\overline{RAS}$ is generated for the memory array. The output buffer is enabled only during an op code fetch or memory read when $\overline{ADDRESS\ DECODE}$, $\overline{MREQ}$, and $\overline{RD}$ are all low. The switch multiplexer signal (MUX) is generated on the rising edge of Φ after $\overline{MREQ}$ has gone low during an op code fetch, memory read or memory write. After MUX is generated and the address multiplexers switch from the row address to column address, $\overline{CAS}$ will be generated. $\overline{CAS}$ comes from one of the outputs of the multiplexer and is delayed by two gate delays to ensure that the proper column address set-up time will be achieved. Once $\overline{RAS}$ and $\overline{CAS}$ have been generated for the memory array, the memory will then access the desired location for a read or write operation.

7404	22ns	Generate $\overline{RAS}$ from $\overline{MREQ}$
7400	15ns	
	63ns	$\overline{RAS}$ to rising edge of Φ
74S74	10ns	Φ to MUX
74S157	15ns	Generate $\overline{CAS}$ from MUX
7404	22ns	
7404	15ns	
t_{CAC}	165ns	$\overline{CAS}$ access time
81LS97	22ns	Output buffer delay
	349ns	Worst case access

DESIGN EXAMPLE NO. 1 MEMORY TIMING
Figure 7



The worst case access time required by the CPU for the op code fetch is 450ns (from equation 1); therefore, the circuit exceeds the required access time by 101ns (worst case).

The circuit shown in Figure 6 provides excellent performance when used as a small on board memory. The memory size should be held at eight devices because there is not sufficient timing margin to allow the interface circuit to drive a larger memory array.

Design Example Number 2: 16Kx8 Memory

This design example describes a 16K/64Kx8 memory which is best suited for a Z80 based microcomputer system where a large amount of RAM is desired. The memory devices used in this example are the same as for the first example, the MK4027 and the MK4116. Again as with the first example, the memory may be expanded from a 16Kx8 to a 64Kx8 by reconfiguring jumpers. See Table 3 and 4 for jumper options.

Figure 8 shows the schematic diagram for the 16K/64K memory. A timing diagram is shown in Figure 9. The operation of the circuit can be described as follows: $\overline{RAS}$ is generated by NANDing MREQ with ADDRESS DECODE (from the two 74LSI38s) + RFSH. Only one row of RAMs will receive a $\overline{RAS}$ during an op code fetch, memory read or memory write. However, an $\overline{RAS}$ will be generated for all rows within the array during a refresh cycle. $\overline{MREQ}$ is inverted and fed into a TTL compatible delay line to generate MUX and $\overline{CAS}$. (This particular approach differs from the method used in example number 1 in that all memory timing is referenced to MREQ, whereas the circuit in example number 1 bases its memory timing from both $\overline{MREQ}$ and the clock. Both methods offer good results; however, the TTL delay line approach offers the best control over the memory timing.) MUX is generated 65ns later and is used to switch the 74157 multiplexers from the row to the column address. The 65ns delay was chosen to allow adequate margin for the row address hold time t_{RAH}. At 110ns, $\overline{CAS}$ is generated from the delay line and NANDed with RFSH, which inhibits a $\overline{CAS}$ during refresh cycle. After $\overline{CAS}$ is applied to the memory, the desired location is then accessed. A worst case access timing analysis for the circuit shown in Figure 8 can be computed as follows:

74LS14	22ns	Generate $\overline{RAS}$ from $\overline{MREQ}$
74LS00	15ns	
delay line	50ns	MUX from $\overline{RAS}$
delay line	45ns	$\overline{CAS}$ delay from MUX
7400	20ns	
t_{CAC}	165ns	Access time from $\overline{CAS}$
8833	30ns	Output buffer delay
	347ns	

The required access time from the CPU is 450ns (from equation 1). This leaves 103ns of margin for additional CPU buffers on the control and address lines. This particular circuit offers excellent results for an application which requires a large amount of RAM memory. As mentioned earlier, the memory timing used in this example offers the best control over the memory timing and would be ideally suited for an application which required direct memory access (DMA).

4K x 8 CONFIGURATION(MK4027) JUMPER

Table 1

CONNECT: J13 to J14

ADDRESS	CONNECT
0000-0FFF	J17 to J25
1000-1FFF	J18 to J25
2000-2FFF	J19 to J25
3000-3FFF	J20 to J25
4000-4FFF	J21 to J25
5000-5FFF	J22 to J25
6000-6FFF	J23 to J25
7000-7FFF	J24 to J25

Connect: J2 to J3
J4 to J6
J7 to J8
J9 to J10
J11 to J12

CONNECT: J14 to J15

ADDRESS	CONNECT
8000-8FFF	J17 to J25
9000-9FFF	J18 to J25
A000-AFFF	J19 to J25
B000-BFFF	J20 to J25
C000-CFFF	J21 to J25
D000-DFFF	J22 to J25
E000-EFFF	J23 to J25
F000-FFFF	J24 to J25

16K x 8 CONFIGURATION (MK4116) JUMPER CONNECTIONS

Table 2

CONNECT:
J1 to J2
J4 to J5
J8 to J11
J10 to J13
J12 to J16
J14 to J16

ADDRESS	CONNECT
0-3FFF	J17 to J25
4000-7FFF	J18 to J25
8000-BFFF	J19 to J25
C000-FFFF	J20 to J25

CONNECT:	J1 to J3
	J5 to J6
	J7 to J8
	J9 to J10
	J11 to J12
	J13 to J14

ADDRESS:	0-3FFF
CONNECT:	J24 to J25
	J26 to J27
	J28 to J29
	J30 to J31

ADDRESS:	4000-7FFF
CONNECT:	J16 to J17
	J18 to J19
	J20 to J21
	J22 to J23

ADDRESS:	8000-BFFF
CONNECT:	J40 to J41
	J42 to J43
	J44 to J43
	J46 to J47

ADDRESS:	C000-FFFF
CONNECT:	J32 to J33
	J34 to J35
	J36 to J37
	J38 to J39

64K x 8 CONFIGURATION(MK4116)

Table 4

CONNECT:	J1 to J2
	J4 to J5
	J8 to J11
	J10 to J13
	J12 to J15
	J14 to J15

ADDRESS: 0-FFFF	
CONNECT:	J32 to J33
	J34 to J35
	J36 to J37
	J38 to J39

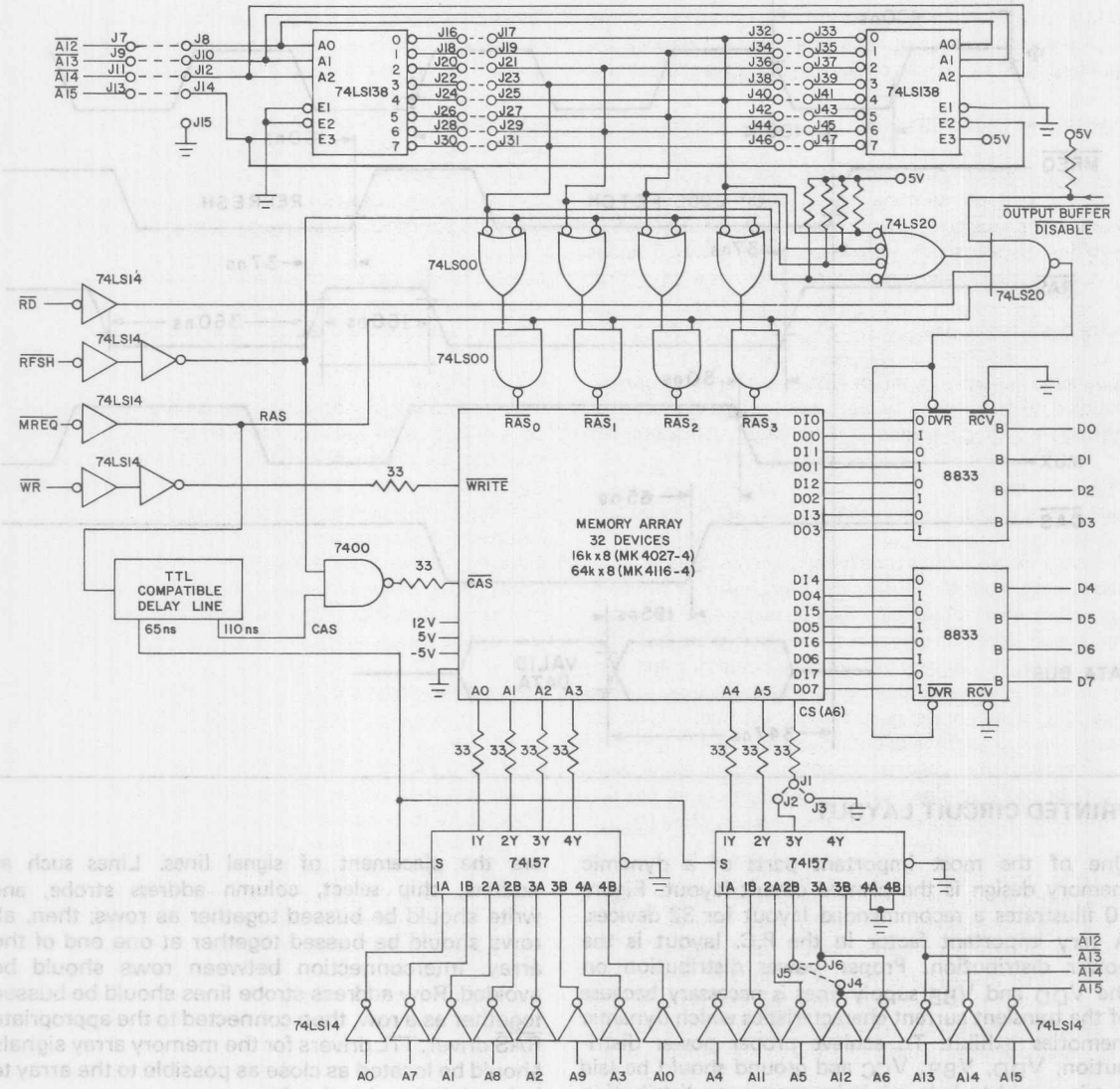
SYSTEM PERFORMANCE CHARACTERISTICS

Table 5

The system characteristics for the preceeding design examples are shown in Table 5.

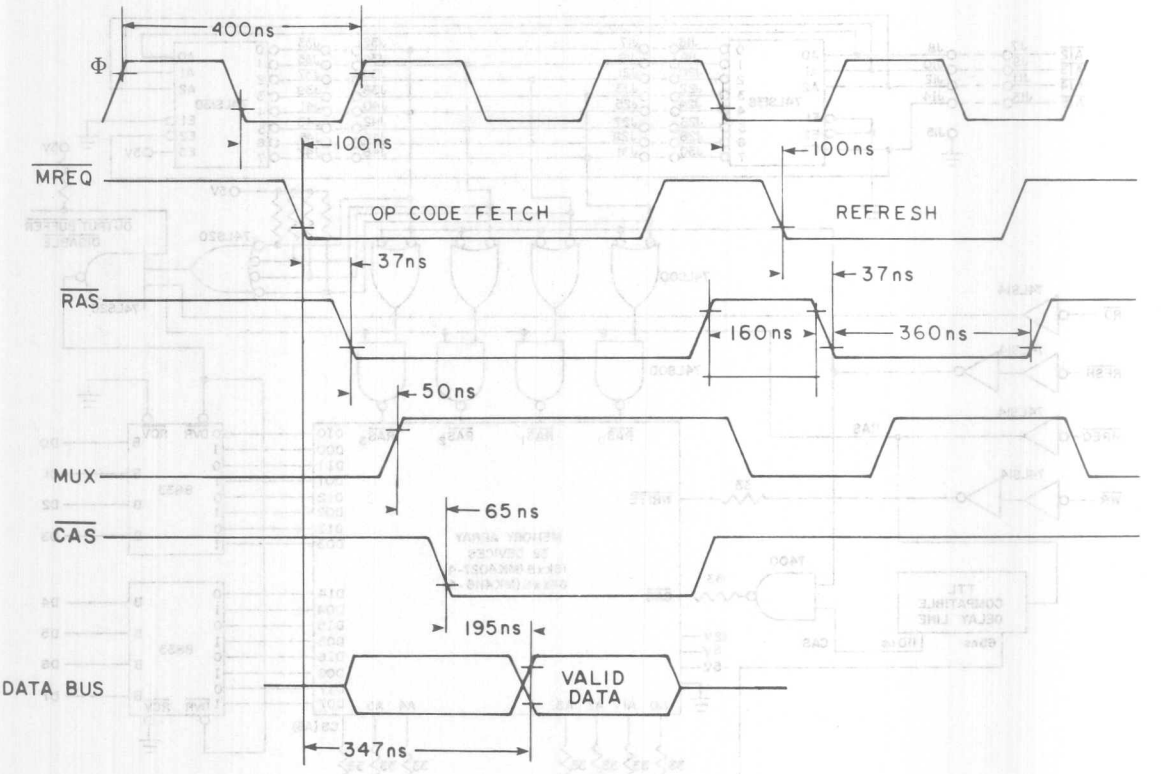
EXAMPLE #	MEMORY CAPACITY	MEMORY ACCESS	POWER REQUIREMENTS
1	4K/16Kx8	349ns max.	+12V @ 0.0250 A max. +5V @ 0.422 A max.* -5V @ 0.030 A max.
2	16K/64Kx8	347ns max.	+12V @ 0.600 A max. +5V @ 0.550 A max. * -5V @ 0.030 A max.

*All power requirements are max.; operating temperature 0°C to 70°C ambient, max +12V current computed with Z80 executing continuous op code fetch cycles from RAM at 1.6 μs intervals.


74LS138
74LS138
74LS00
74LS00
74LS20
74LS20
74LS14
74LS14
74LS14
74LS14
74LS14
74LS14
74LS14
74LS14
OUTPUT BUFFER DISABLE
5V
5V
RD
RFSH
MREQ
WR
RAS
33
WRITE
CAS
7400
TTL COMPATIBLE DELAY LINE
65ns
110ns
CAS
12V
5V
-5V
MEMORY ARRAY
32 DEVICES
16k x 8 (MK4027-4)
64k x 8 (MK4116-4)
8833
8833
CS (A6)
74157
74157
FOR JUMPER OPTIONS SEE TABLES 3 AND 4

DESIGN EXAMPLE NO. 2 MEMORY TIMING

Figure 9



PRINTED CIRCUIT LAYOUT

One of the most important parts of a dynamic memory design is the printed circuit layout. Figure 10 illustrates a recommended layout for 32 devices. A very important factor in the P.C. layout is the power distribution. Proper power distribution on the V_{DD} and V_{BB} supply lines is necessary because of the transient current characteristics which dynamic memories exhibit. To achieve proper power distribution, V_{DD}, V_{BB}, V_{CC} and ground should be laid out in a grid to help minimize the power distribution impedance. Along with good power distribution, adequate capacitive bypassing for each device in the memory array is necessary. In addition to the individual by-passing capacitors, it is recommended that each supply (V_{BB}, V_{CC} and V_{DD}) be bypassed with an electrolytic capacitor 20μF.

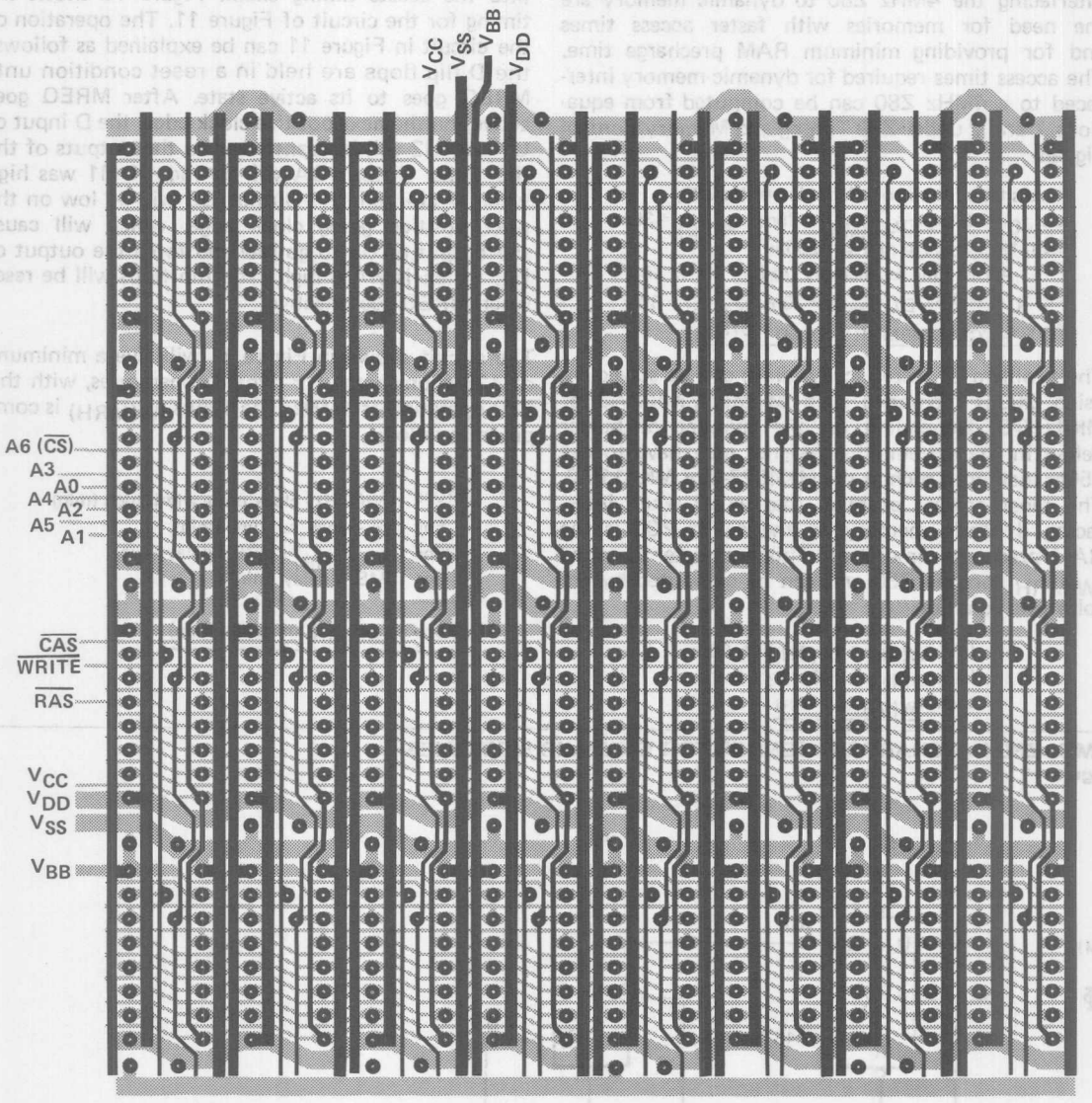
By using good power distribution techniques and using the recommended number of bypassing capacitors, the designer can minimize the amount of noise in the memory array. Other layout considerations are the placement of signal lines. Lines such as address, chip select, column address strobe, and write should be bussed together as rows; then, all rows should be bussed together at one end of the array. Interconnection between rows should be avoided. Row address strobe lines should be bussed together as a row, then connected to the appropriate $\overline{RAS}$ driver. TTL drivers for the memory array signals should be located as close as possible to the array to help minimize signal noise.

For a large memory array such as the one shown in design example number 2, series terminating resistors should be used to minimize the amount of negative undershoot. These resistors should be used on the address lines, $\overline{CAS}$ and $\overline{WRITE}$, and have values between 20 Ω to a 33 Ω .

The layout for a 32 device array can be put in a 5" x 5" area on a two sided printed circuit board.

SUGGESTED P. C. LAYOUT FOR MK4027 or MK4116

Figure 10



III

A 4MHz Z80 is available for the microcomputer designer who needs higher system throughput. Considerations which must be faced by the designer when interfacing the 4MHz Z80 to dynamic memory are the need for memories with faster access times and for providing minimum RAM precharge time. The access times required for dynamic memory interfaced to a 4MHz Z80 can be computed from equations 1 and 2 under Z80 Timing and Memory Control Signals.

Access time for op code fetch for 4MHz Z80,
let: $t_C = 250ns$; $t_{DL\overline{\Phi}(MR)} = 75ns$; $t_{s\overline{\Phi}(D)} = 35ns$
then: $t_{ACCESS\ OP\ CODE} = 265ns$

Access time for memory read for 4MHz Z80,
let: $t_C = 250ns$; $t_{DL\overline{\Phi}(MR)} = 75ns$; $t_{S\overline{\Phi}(D)} = 50ns$
then: $t_{ACCESS\ MEMORY\ READ} = 375ns$

The problem of faster access times can be solved by using 200ns memories such as the MK4027-3 or MK4116-3. Depending on the number of buffer delays in the system, the designer may have to use 150ns memories such as the MK4027-2 or MK4116-2. The most critical problem that exists when interfacing dynamic memory to the 4MHz Z80 is the RAM precharge time (trp). This parameter is called $t_{W(MRH)}$ on the Z80 and can be computed by the following equation.

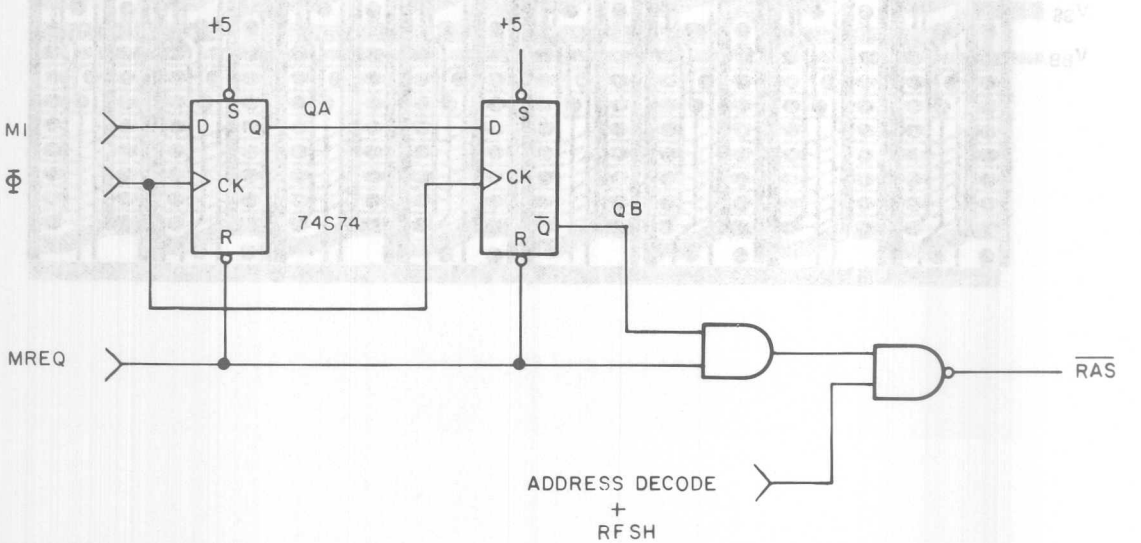
(4) $t_{W(RH)} = t_{W(\Phi H)} + t_f - 20ns$
let: $t_{W(\Phi H)} = 110ns$; $t_f = 5ns$
then: $t_{W(MRH)} = 95ns$

120ns precharge. Figure 11 shows a circuit that will lengthen the $t_{W(MRH)}$ pulse from 95ns to a minimum of 126ns while only inserting one gate delay into the access timing chain. Figure 12 shows the timing for the circuit of Figure 11. The operation of the circuit in Figure 11 can be explained as follows: the D flip flops are held in a reset condition until MREQ goes to its active state. After MREQ goes active, on the next positive clock edge, the D input of U1 and U2 will be transferred to the outputs of the flip flops. Output QA will go high if M1 was high when Φ clocked U1. Output QB will go low on the next positive going clock edge, which will cause the output of U3 to go low and force the output of U4, which is $\overline{RAS}$, high. The flip flops will be reset when MREQ goes inactive.

The circuit shown in Figure 11 will give a minimum of 126ns precharge for dynamic memories, with the Z80 operating at 4MHz. The 126ns $t_{W(MRH)}$ is computed as follows.

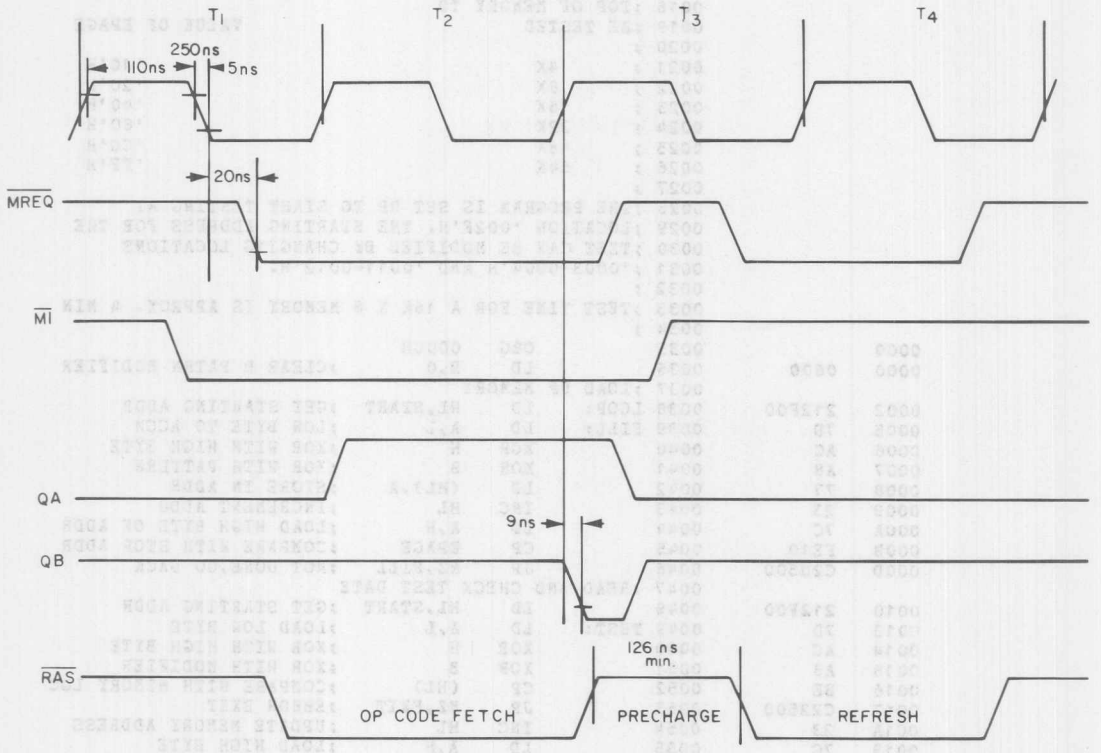
110ns	$t_{W(\Phi H)}$ - clock pulse width high (min)
5ns	t_F - clock full time (min)
20ns	$t_{DL\overline{\Phi}(MR)}$ - MREQ delay (min)
-9ns	74S74 delay (min)
126ns	$t_{W(MRH)}$ modified (min)

4MHz Z80 PRECHARGE EXTENDER FOR DYNAMIC MEMORIES
Figure 11



TIMING DIAGRAM FOR 4MHz Z80 PRECHARGE EXTENDER

Figure 12



III

APPENDIX

MEMORY TEST ROUTINE

This section is intended to give the microcomputer designer a memory diagnostic suitable for testing memory systems such as the ones shown in Section VI.

The routine is a modified address storage test with an incrementing pattern. A complete test requires 256_{10} passes, which will execute in less than 4 minutes for a 16Kx8 memory. If an error occurs, the program will store the pattern in location '2C'H and the address of the error at locations '2D'H and '2E'H.

The program is set up to test memory starting at location '2F'H up to the end of the block of memory defined by the bytes located at 'OC'H and 'OD'H. The test may be set up to start at any location by modifying locations '03'H - '04'H and '11'H - '12'H with the starting address that is desired.

```
                          MXRTS  LISTING                    PAGE  0001
     LOC   OBJ CODE   STMT SOURCE STATEMENT

                      0001 ;TRANSLATED FROM DEC 1976 INTERFACE MAGAZINE
                      0002 ;
                      0003 ;THIS IS A MODIFIED ADDRESS STORAGE TEST WITH AN
                      0004 ;INCREMENTING PATTERN
                      0005 ;
                      0006 ;256 PASSES MUST BE EXECUTED BEFORE THE MEMORY IS
                      0007 ;COMPLETELY TESTED.
                      0008 ;
                      0009 ;IF AN ERROR OCCURS, THE PATTERN WILL BE STORED
                      0010 ;AT LOCATION '002C'H AND THE ADDRESS OF THE
                      0011 ;ERROR LOCATION WILL BE STORED AT '002D'H AND
                      0012 ;'002E'H.
                      0013 ;
```

MEMORY TEST ROUTINE (Cont'd.)

```
                        0014 ;THE CONTENTS OF LOCATIONS '000C'H AND '001D'H
                        0015 ;SHOULD BE SELECTED ACCORDING TO THE FOLLOWING
                        0016 ;MEMORY SIZE TO BE TESTED
                        0017 ;
                        0018 ;TOP OF MEMORY TO
                        0019 ;BE TESTED                          VALUE OF EPAGE
                        0020 ;
                        0021 ;      4K                                  '10'H
                        0022 ;      8K                                  '20'H
                        0023 ;     16K                                  '40'H
                        0024 ;     32K                                  '80'H
                        0025 ;     48K                                  'C0'H
                        0026 ;     64K                                  'FF'H
                        0027 ;
                        0028 ;THE PROGRAM IS SET UP TO START TESTING AT
                        0029 ;LOCATION '002F'H. THE STARTING ADDRESS FOR THE
                        0030 ;TEST CAN BE MODIFIED BY CHANGING LOCATIONS
                        0031 ;'0003-0004'H AND '0011-0012'H.
                        0032 ;
                        0033 ;TEST TIME FOR A 16K X 8 MEMORY IS APPROX. 4 MIN
                        0034 ;
0000                    0035          ORG   0000H
0000  0600              0036          LD    B,0          ;CLEAR B PATRN MODIFIER
                        0037 ;LOAD UP MEMORY
0002  212F00            0038 LOOP:    LD    HL,START     ;GET STARTING ADDR
0005  7D                0039 FILL:    LD    A,L          ;LOW BYTE TO ACCM
0006  AC                0040          XOR   H            ;XOR WITH HIGH BYTE
0007  A8                0041          XOR   B            ;XOR WITH PATTERN
0008  77                0042          LD    (HL),A       ;STORE IN ADDR
0009  23                0043          INC   HL           ;INCREMENT ADDR
000A  7C                0044          LD    A,H          ;LOAD HIGH BYTE OF ADDR
000B  FE10              0045          CP    EPAGE        ;COMPARE WITH STOP ADDR
000D  C20500            0046          JP    NZ,FILL      ;NOT DONE,GO BACK
                        0047 ;READ AND CHECK TEST DATE
0010  212F00            0048          LD    HL,START     ;GET STARTING ADDR
0013  7D                0049 TEST:    LD    A,L          ;LOAD LOW BYTE
0014  AC                0050          XOR   H            ;XOR WITH HIGH BYTE
0015  A8                0051          XOR   B            ;XOR WITH MODIFIER
0016  BE                0052          CP    (HL)         ;COMPARE WITH MEMORY LOC
0017  C22500            0053          JP    NZ,FXIT      ;ERROR EXIT
001A  23                0054          INC   HL           ;UPDATE MEMORY ADDRESS
001B  7C                0055          LD    A,H          ;LOAD HIGH BYTE
001C  FE10              0056          CP    EPAGE        ;COMPARE WITH STOP ADDR
001E  C21300            0057          JP    NZ,TEST      ;LOOP BACK
0021  04                0058          INC   B            ;UPDATE MODIFIER
```

```
                                MXRTS  LISTING                    PAGE   0002
 LOC   OBJ CODE   STMT SOURCE STATEMENT
0022  C30200            0059          JP    LOOP         ;RST WITH NEW MODIFIER
                        0060 ;ERROR EXIT
0025  222D00            0061 FXIT:    LD    (BYTE),HL    ;SAVE ERROR ADDRESS
0028  322C00            0062          LD    (PATRN),A    ;SAVE BAD PATTERN
002B  76                0063          HALT               ;FLAG OPERATOR
002C                    0064 PATRN:   DEFS  1
002D                    0065 BYTE:    DEFS  2
002F  2F00              0066 START:   DEFW  $
                        0068 EPAGE:   EQU   10H          ;SET UP FOR 4K TEST
                        0069          END
```

ABSTRACT

This paper discusses the evolution of dynamic MOS RAMs. Included is a discussion of address multiplexing and timing considerations of multiplexed address MOS RAMs. Static and dynamic sense amplifiers are compared in terms of power consumption and layout problems and the benefits resulting from the use of dynamic sense amplifiers are discussed.

INTRODUCTION

Semiconductor random access memories have been developed at a very rapid pace throughout this decade. RAMs with very impressive performance have been produced using bipolar technology, while RAMs with moderate performance but very low cost have been produced using MOS technology. This paper will discuss dynamic MOS random access memories which have replaced core memories in most memory applications. This recent dominance by dynamic MOS RAMs in the random access memory market comes about as a result of the cost, performance, and reliability associated with the integration of up to 65,536 bits of RAM on a single integrated circuit. This level of integration in turn is made possible by the use of dynamic circuit techniques, and more specifically by the use of dynamic data storage. These techniques have undergone very rapid development, causing the performance characteristics of available memory circuits to vary greatly from design to design as different techniques are incorporated. Dynamic and static sense amplifiers will be discussed, and the performance specifications of a commercially available 16 K RAM using dynamic sense amplifiers will be compared to the specifications of two 16 K RAMs using static sense amplifiers. The state-of-the-art in commercially available MOS memory is a 64 K x 1 dynamic circuit with a chip access time of 150 nanoseconds, and a read-modify-write cycle time of 310 nanoseconds. Cost of dynamic MOS memory is rapidly decreasing and is now about 0.03 cent per bit at the chip level and about 0.08 cent per bit at the system level.

DEVELOPMENT OF DYNAMIC MEMORY

The first MOS RAMs used cross-coupled flip-flops as storage cells, each cell containing six or eight MOS transistors. The combination of a complex cell structure and a new technology gave rise to a high per-bit memory cost that found very few applications. But applications were expanded by major breakthroughs that significantly reduced the cost of MOS RAM. The first breakthrough was the development of the concept of dynamic memory storage — storing a digital "0" or "1" by a low or high voltage stored on a capacitor in a 3-transistor cell. However, this can cause a problem since the charge will eventually leak off any capacitor. If data is to be retained for longer than the self discharge time of a cell storage capacitor, typically two milliseconds, the data must be sensed before it is lost and then restored to its original voltage level. The operation of restoring the cell voltages to good levels is called a refresh operation. This simultaneously occurs in all cells of the externally addressed row of the memory matrix. To refresh the entire memory array, it is necessary to perform a refresh cycle to each of the rows of the memory array at least once every two milliseconds.

The second major breakthrough in the development of MOS RAMs was the development of the single transistor cell. This cell is poorly named because it really consists of a single transistor plus a single capacitor, and the capacitor occupies the majority of the cell area. But this cell still occupied less than half the area of the earlier 3-transistor cell and permitted integration of 4096 bits per chip compared to only 1024 bits per chip using the earlier 3-transistor cell. The three year delay between the introduction of the 1-transistor cell was due to the difficulty in sensing the small signal from the 1-transistor cell. For the first time, there was no amplifier built into every cell, and signal levels out of the memory matrix became millivolts instead of volts. Sense amplifiers have been developed to sense the small signals from the 1-transistor cell and will be discussed later.

The 1-transistor cell permitted integration of 4 K bits per chip. In addition, improvements in the internal peripheral or support circuits made this new generation of circuits much easier to use than were the earlier 1 K circuits. The 1 K circuits required multiple, critically-timed, high-capacitance, high-voltage clock signals. In the 4 K chips, these were replaced by a single high-voltage, high-capacitance clock (22 pin version) or two TTL-level, low-capacitance clocks for address and data inputs, which were replaced by TTL-level inputs in the 4 K chips. The high impedance output of the 1 K chips, requiring an external sense amplifier, was replaced by a low impedance output capable of driving one or more TTL loads in the 4 K circuits. The relatively slow P-channel technology used for the 1 K chips was replaced by faster N-channel technology for the 4 K chips. Integration of 4096 bits per chip reduced the per-bit chip cost, while the simplification of external support circuitry reduced other

general applications. The 16 K devices introduced in 1973 continued the trend. Integration of 64 K bits per chip promises to reduce the per-bit cost even further.

In order to achieve 64 K density, scaled processing was required. The scaled devices were able to use a single +5 volt power supply rather than the multiple supplies used by the previous generations. The single supply requirement greatly simplifies system design.

Although 64 K chips require approximately the same external circuitry, a given printed circuit board and system circuitry supports 4 times as many bits as when using 16 K chips.

ADDRESS MULTIPLEXING

While use of the single transistor cell increased the bit density on a chip, it degraded the access time by about 25 percent. This is due to the delay through the sense amplifiers in detecting and amplifying the very small signals from the memory cells. This delay, however, made the multiplexing of addresses a very attractive means for reducing package pin count for increased memory density on a printed circuit board.

An MOS memory chip is physically arranged as a two dimentional array of cells. Certain address inputs are used for row selection and the remaining address inputs are used for column selection. Row selection is required before the sense amplifiers can begin their slow detection process. Column selection is not required until the outputs of the sense amplifiers are valid, since its function is to gate data from the selected sense amplifier to the data output circuitry. Since the column selection information is not used internally until well after the row selection information is required, only the row addresses need to be available to the chip at the start of a cycle. The column address can come later with no penalty of access time. The multiplexed address memory takes advantage of this delayed need for column address. Instead of using 12 address pins to select one of 4096 memory cells, six address pins are used to first select one of 64 rows, and subsequently the same pins are used to select one of 64 columns. The result is a 4096 bit RAM in a 16 pin package, rather than in the more straightforward 22 pin package.

When compared to the 22 pin 4 K RAM, the 16 pin 4 K RAM has both advantages and disadvantages. The primary advantage of the 16 pin approach is the substantial increase in board density that it allows. A second advantage is the halving the required number of address buffers. A third advantage is that multiplexing permits a faster mode of operation, called page mode, which shall be discussed later. Finally, two more specific advantages were available to users of the 16 pin design. These were the use of TTL-level timing signals rather than a high voltage clock, and the use of dynamic sense amplifiers rather than static sense nevertheless, advantageous for users of the 16 pin design.

The 16 pin implementation also had disadvantages. The multiplexed part required two timing signals and hence more complex timing. The first signal, $\overline{RAS}$, initiates a cycle and strobes in the row address, and the second signal, $\overline{CAS}$, strobes in the column address. Any skew in the timing of the second signal with respect to the first added directly to access time. Systems using the 22 pin design, which required only a single clock, had less complex timing and suffered no such degradation of access time. Finally, the 22 pin design, not having the TTL to MOS level clock driver on the chip, dissipated less than 1 mW in the standby mode compared to about 10 mW per chip for the 16 pin part.

In the first year after various designs were introduced, the 22 pin approach gained greater acceptance than the 16 pin approach, not because of the technical advantages or disadvantages of the two approaches, but because there were two major MOS memory suppliers manufacturing the 22 pin part and only one manufacturing the 16 pin part. Many users would not choose a single-sourced product. Other users had a strong enough preference for the multiplexed concept to commit to that design, correctly assuming that the market they created for the 16 pin design would cause additional manufacturers to offer their own 16 pin designs. Meanwhile, the 16 pin design was improved to eliminate the access time penalty due to multiplexing. This was accomplished by performing the critical timing of the second clock with circuitry on the chip rather than with external circuitry—a feature referred to as "gated $\overline{CAS}$." With many users committed to a multiplexed design, other manufacturers began supplying this part. And with multiple sourcing available, more and more users designed systems using the 16 pin part. This trend has escalated to the point where all new memory system designs now incorporate the 16 pin device.

The acceptance of address multiplexing generated by 4K RAMs virtually assured its use in the next generation of dynamic MOS RAMs. And indeed all 64 K RAMs on the market today use address multiplexing and are pin compatible with each other. The JEDEC approved standard for the propsed 256 K RAM is also in the 16 pin package. Many new memory system designs take advantage of the pinout similarity between the 4 K, 16 K, and 64 K parts. Printed circuit boards are designed to accommodate any of the parts.

MULTIPLEX TIMING CONSIDERATIONS

Although address multiplexing provides some very substantial system benefits, it complicated system timing. It requires that both row and column addresses get into the chip in a short time using the same address pins. This establishes a rather tight timing window during which the individual events must occur. The sequence of events required to address the chip is as follows: (1) establish row

specified access time from $\overline{RAS}$, it is necessary to bring $\overline{CAS}$ low within some specified maximum delay after $\overline{RAS}$.

Every attempt is made during the design of multiplexed chips to simplify the system timing problem. This is done by first reducing the row address hold time to an absolute minimum, since the system must not begin to establish column addresses until the minimum row address hold time is met. This also increases the time available for multiplexing. Finally, the critical $\overline{RAS}$ to $\overline{CAS}$ timing is done on the chip, which means that if $\overline{CAS}$ occurs earlier than needed by the chip, it is internally delayed until it is needed ("gated $\overline{CAS}$"). For high performance memory systems, the use of a delay line to minimize timing skews is essential. With a delay line, the timing sequence can be met such that $\overline{CAS}$ occurs early enough after $\overline{RAS}$ to guarantee the specified access time from $\overline{RAS}$.

OPERATION OF MULTIPLEXED DYNAMIC RAMS

In a multiplexed design, the 12 addresses of a 4 K memory, the 14 addresses of a 16 K memory, or the 16 addresses of a 64 K memory are strobed into the memory chip in two groups of 6, 7, or 8 respectively. When an address becomes available for a memory operation, the row address must first be presented to the chip address pins. As soon as the row address inputs are valid, the first of two timing signals to the chip initiates a cycle. This signal strobes or latches the row address into the chip and is appropriately called Row Address Strobe or $\overline{RAS}$. With no further commands to the chip, the latched addresses are converted to MOS voltage levels, decoded, and the selected row is enabled. Data is thereby destructively read from each cell in the selected row by dumping its charge onto is respective column sense line. A sense amplifier for each column detects the change in voltage level on the column line resulting from this deposited charge, and amplifies this signal. The amplified signals from the sense amplifiers are then impressed back onto the column sense lines, returning the cells to their original voltages. A cell whose voltage had decayed is restored to its original voltage in the prcoess. At this time the sense amplifiers contain the same data or information contained in the selected row, and the destructively-read cells in the row are restored (refreshed) to their proper voltage.

When an active cycle is initiated by $\overline{RAS}$ going low, it must not be aborted. It is necessary to keep $\overline{RAS}$ low for some minimum length of time to allow the sense amplifiers time to restore data back into the destructively-read cells. To summarize, the function of the Row Address Strobe is to initiate a cycle, strobe or latch the row address, enable the selected row of memory cells, and maintain the sensed data from the entire row of addressed memory cells in their respective sense amplifiers. The sense amplifiers maintain this data as long as $\overline{RAS}$ remains active. At the end of a

The Column Address Strobe ($\overline{CAS}$), on the other hand, controls column selection circuitry and the transfer of data from the selected sense amplifier to the output circuitry. After $\overline{RAS}$ strobes the row address information from the multiplexed address input pins, $\overline{CAS}$ strobes the column address from the same pins. When $\overline{CAS}$ goes active (low), the column address is strobed or latched into the circuit. This address is then decoded to select the proper column. Data from the selected sense amplifier is then transferred to the output buffer, completing read access.

During a write operation, the same sequence of events occurs as in a read cycle, with identically the same timing as in a read cycle except that the write enable signal, $\overline{WRITE}$, is brought active (low). This causes the data at the data input to be strobed into the chip, buffered, and written into the selected sense amplifier and, thereby, into the selected cell. A read-modify-write cycle starts out as a read cycle until read access time. Then when input data becomes available to the memory, $\overline{WRITE}$ must be activated. As in a write-only cycle, this causes the data to be written into both the selected sense amplifier and into the selected cell. The active cycle must not be terminated until the internal write circuitry has had sufficient time to complete the write operation.

PAGE MODE PERATION

The Row Address Strobe transfers the data from an entire row of memory cells into their respective sense amplifiers. The Column Address Strobe transfers the single bit of data from the selected sense amplifiers into the output buffer. This organization permits data to be transferred into or out of multiple column locations of the same row by having multiple column cycles during a single active row cycle. This mode of operation is called page mode. A page of memory is defined as those memory locations sharing a common row address, but not necessarily confined to a single chip.

After a row has been selected by the Row Address Strobe, the contents of all cells in that row are available in their respective sense amplifiers. Repetitive column address cycles, while maintaining a single active row cycle, permit faster operation than is possible in the normal operating mode. This is because the delay through the sense amplifier only adds to the access time of the first column in the page. Data to be accessed from each subsequent column is already available in its respective sense amplifier. Therefore, page mode access is the access time from $\overline{CAS}$, which is typically two-thirds the access time from $\overline{RAS}$. Page mode reduces power consumption while typically doubling maximum operating frequency. Read, write, and read-modify-write cycles can be performed in either normal cycles or in page cycles. Page mode operation has a number of applications, with high-speed block transfer of data being

the most important.

SENSE AMPLIFIER CONSIDERATIONS

The one-transistor memory cell has been simplified to a rather minimal structure: a capacitor stores digital data as a high or low voltage, and a transistor selectively connects the capacitor to a digit/sense line. (See Fig. 1.) Conduction through the transistor is controlled by its gate which is electrically connected to the other gates in a row. When a row is enabled by the row decoder, all transistors in that row become conductive, transferring charge from their respective capacitors to their respective digit/sense lines, destructively reading data. Each column has its own sense amplifier, whose function is to detect this charge and to amplify the signal caused by this charge. The amplified signal is a full logic level, either at ground or close to V_{DD}.

The cell transistors remain conductive throughout this period so that the amplified signals from the sense amplifiers feed back into their respective cells, refreshing the voltage levels in the cells.

To maximize the signal into the sense amplifier, a large cell capacitance and a small digit/sense line capacitance are desired. This is because the cell and its digit line form a capacitive divider that attenuates the signal from the cell. But integration of large numbers of bits on one circuit requires a physically small cell size which implies an electrically small cell capacitance. Integration of large numbers of bits also requires that many cells share a common digit/sense line, causing this line to be physically long and to therefore have high stray capacitance. To keep the signal attenuation to an acceptable level, steps are taken to both maximize cell capacitance and to minimize digit line capacitance. Cell capacitance can be increased by using a double layer polysilicon fabrication process, which increases the percentage of cell area used for the capacitor. Digit line capacitance can be reduced by simply cutting the line in half. The sense amplifier is then placed in the center of a digit line, and senses a differential voltage between the two halves of the line. In 16 K designs, the cell capacitance is typically 0.04 picofarad and the stray capacitance of one half-digit is typically 1 picofarad. Thus the signal from the memory cell is attenuated by a factor of 25 before being sensed by the sense amplifier. At the 64 K level, substituting polysilicon digit lines for the diffused digit lines used on the 16 K has reduced the attenuation factor to approximately 14.

Between cycles, the two halves of each digit line are equilibrated to precisely the same voltage. When an active cycle is initiated by $\overline{RAS}$ going low, these lines are momentarily allowed to float. Then a row is enabled, transferring charge from the enabled cell in each column to its half of its digit line. On each digit line, only a single memory cell is selected. This cell may be located on either the top or bottom half of the digit line. If the cell was originally at a high voltage, it causes its half-digit line voltage to be at some "high" value. If the cell was originally at a low voltage, its resulting half-digit line voltage is some "low" value. It should be noted that the attenuation of the digit line causes the "high" and "low" voltages to differ by less than one-half volt. The half-digit line not containing the addressed cell is simultaneously adjusted to a reference voltage somewhere between the "high" and "low" voltages of the addressed half by using dummy cells in the 4 K and 16 K RAMs. At the 64 K level, Mostek has used a digit line precharging scheme which has eliminated the necessary of a dummy cell. Thus if a cell originally contained a high voltage, the voltage of its half-digit line will be approximately one-quarter volt above the adjusted intermediate voltage of the other half-digit line. If the cell originally contained a low voltage, the voltage of its half-digit line will be approximately one-quarter volt below the intermediate voltage of the other half-digit line. It is now up to the same amplifier to detect this differential signal of one-quarter volt or less.

A detailed analysis of the sense amplifier will not be attempted. It will simply be noted that the sense amplifier consists of a balanced flip-flop. Since the addressed cell, in conjunction with the dummy cell (4 K and 16 K) guarantees an inital voltage imbalance to this flip-flop, the positive feedback of the flip-flop causes initial voltage remains near V_{DD} for the 4 K and 16 K devices and near the reference voltage for the 64 K device.

Two types of sense amplifiers have been used in commercially available products. These are variations of the static amplifier in Fig. 1, and of the dynamic amplifier in Fig. 2. Both are about equal in their ability to detect and amplify small signals. The load resistors, R1 and R2, in the static amplifiers consume a substantial amount of power, typically half or more of the total chip power. Since these resistors are not present in dynamic amplifiers, the total power consumption of memory chips employing dynamic sense amplifiers is much less than that of circuits employing static sense amplifiers. There are, however, formidable design or layout problems associated with the use of dynamic sense amplifiers which will be discussed presently. These problems are severe enough that many chip designers chose to incorporate power-consuming static sense amplifiers into their designs.

To understand the differing circuit requirements for static and dynamic sense amplifiers, one must look at a write cycle or more accurately, a read-modify-write cycle. Suppose, In Fig. 1, cell 64 had or originally stored a low voltage and was read. The sense amplifier, detecting a lower voltage on node B than on node A, will drive node B to ground and node A near V_{DD}. Transistor T3 then turns on, and the data from the cell becomes available to the output buffer at one end of the data bus. Now, assume that it is desired to write opposite data back into the cell. This requires forcing a high voltage onto node B and onto the storage capacitor, C64. To do this, the data input buffer will drive the input/output data bus to ground. Transistor T3 then forces node A to ground, overpowering R1. When node A goes to ground, transistor T2 gurns off. This allows R2 to pull node B to V_{DD} as required to write the high level into the storage cell. Without R2, node B would simply remain at

MEMORY CELLS AND STATIC SENSE AMPLIFIER

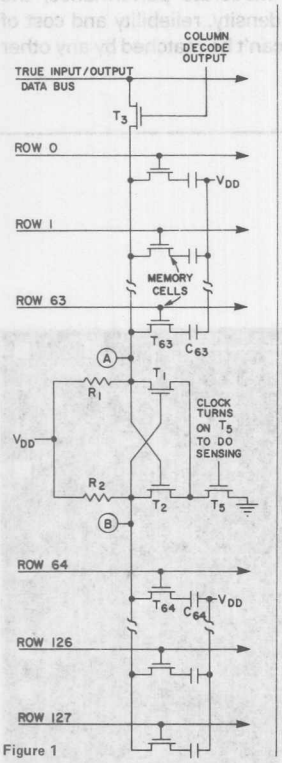


Figure 1

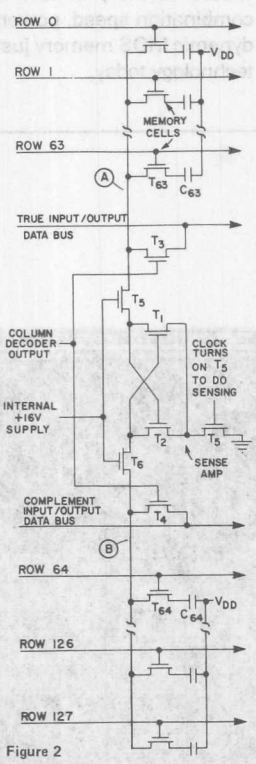


Figure 2

Figure 1 Memory Cells and Static Sense Apmlifier. Memory chips using static sense amplifiers consume twice the power of chips using dynamic sense amplifiers, due to the conduction through either R1 or R2.

Figure 2 Memory Cells and Dynamic Sense Amplifier. The use of dynamic sense amplifiers requires both true and complement input/output data busses. This, in turn, requires either two full column decoders or placement of a single column decoder with the sense amplifiers in the center of the memory.

ground, and a high voltage could not have been written into the cell. With these resistors, data can be written into a cell in either half of the matrix with a single input/output data bus. A trade-off exists in the resistance value chosen for R1 and R2. Since either R1 or R2 will dissipate power in all of the sense amplifiers, a low value resistor results in a very high power consumption. But the digit line capacitance of node B is quite large, and a high value resistor means an excessively long write time. There is no good compromise, circuits using static sense amplifiers consume high power and have long write times.

On paper, the dynamic sense amplifer solves the problem very well. Referring now to Fig. 2 and having again read a low voltage from cell 64, assume it is again desired to write a high voltage back into the cell. Now, as before, the input buffer drives the true data bus to ground, with transistor T3 causing node A to follow. But, in addition the input buffer also forces the complement data bus to V_{DD}, with transistor T4 causing node B to follow. In forcing node B to V_{DD}, the complement data bus performed the job previously done by the resistor. With row 64 still selected, the high voltage on node B is transferred into the cell, and the write operation is complete. It should be noted that transistors T3 and T4 function only as switches and can have very low resistances to speed-up write time. No speed-power trade-off is involved. Therefore, memory designs using dynamic sense amplifiers consume far less power and write much faster than do designs using static sense amplifiers.

The layout problem associated with the dynamic sense amplifier is that it requires both a true and a complement data bus. These, in turn, require that the column decode outputs be available in both the top and bottom halves of the memory array. Placing single column decoder above (or below) the memory array is ruled out since it is not practical to run its outputs through the memory array to the other side. One solution to the layout problem is to use two entire column decoders, one above the top half of the array to service the true data bus, and the other below the bottom half of the array to service the complement data bus. This gains all the advantages of using dynamic sense amplifiers, but the duplication of the column decoder consumes an additional amount of silicon area.

A second solution is to use a single column decoder located in the center of the memory array along with the sense amplifiers. This approach requires great care in design. If the column decoder is located in the center of the chip, it is topologically necessary for the digit lines to cross the buffered column address signals. Just one address signal, moving from ground to V_{DD}, capacitively couples more signal onto a digit line than that provided by the memory cell. At first thought, this is frightening indeed. But on second thought, there are 127 unselected row lines that cross the digit lines and they do not cause a problem. They are quiet. Indeed if all lines crossing the digit line are kept quiet until the sense amplifier detects and amplifies its signal, there is no problem. With a multiplexed design, it is particularly easy to insure that the buffered column address lines remain quiet during this time, since multiplexing automatically causes the column address to be processed after the row addresses have been processed.

The advantages of dynamic sense amplifiers over static sense amplifiers are rather dramatic. Static sense amplifier designs require approximately twice the power of an equivalent dynamic circuit.

CONCLUSION

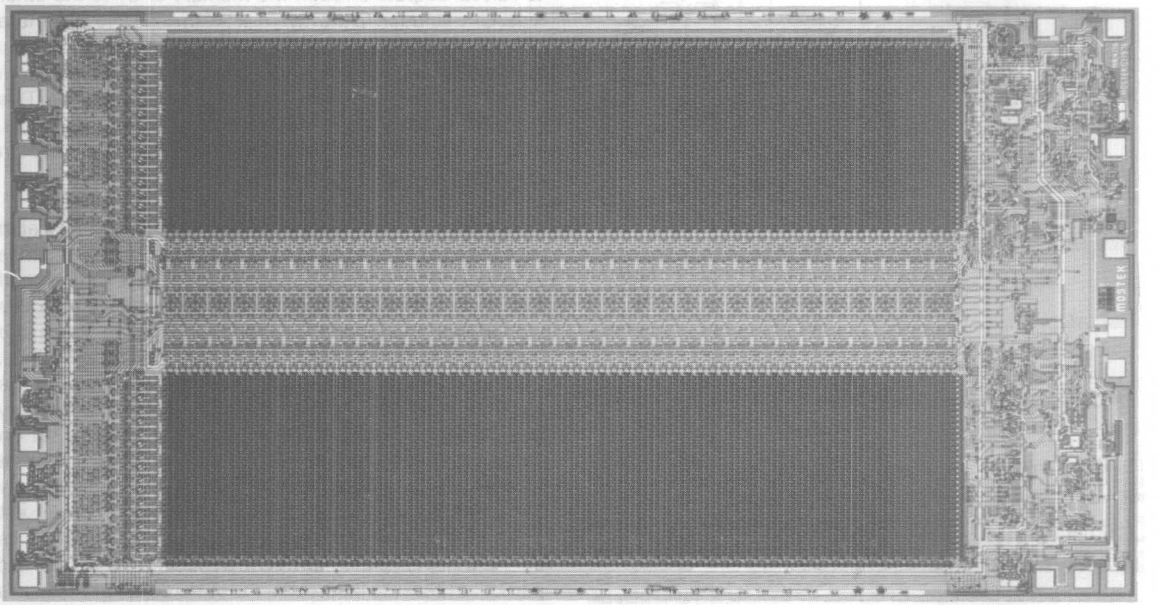
Some of the dynamic MOS RAMs on the market today consume considerably less power than others. Some are considerably faster than others. But compared to other technologies, all of these parts represent very attractive building blocks for random access memory systems.

The high storage density resulting from the use of small 16 pin packages, each containing 64 K bits, is very important in the design of large memory systems. The combination of TTL compatibility of all inputs and outputs, and relatively straightforward timing requirements make these circuits

technology provides the best answer. In systems tolerant of relatively slow serial access rather than requiring fast random access, other technologies, including disc, CCD, or

dynamic MOS memory just can't be matched by any other technology today.

CHIP PHOTOGRAPH OF MK4564
Figure 3



INTRODUCTION

Memory Systems design is very much like any other interface design. It requires knowledge of the system being interfaced to and also an in-depth knowledge of the resource being interfaced. This in-depth knowledge must include the functional and electrical characteristics of the device as well as power requirement, noise sensitivities and driver requirements. This application note will attempt to cover all of the areas that are relevant to designing a memory system using the MK4027 or the MK4116. The discussion centers around a memory board that was designed for the LSI-11* microcomputer. Many of the techniques and methods used in this design can be applied to amost any other memory system design.

THE LSI-11* BUS

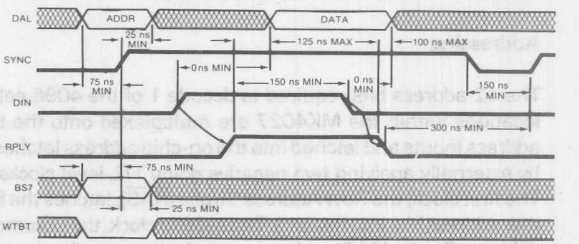
The LSI-11* microcmputer bus is used for all data transfers within the system. It has four types of cycles that are of significance to the memory system: read, write, read-modify-write and refresh. The timing for each of these cycles as seen from the interface side of the bus receivers is given in Figs. 1, 2, and 3. Since the memory can never institute a bus cycle it is always a slave device. As can be seen from the timing diagrams, all cycles are interlocked asynchronous. The bus cycles have three phases; device selection, transfer initiation and transfer termination. Device selection (either memory or peripheral) is accomplished by the bus master placing the device address on the multiplexed address-data lines. After allowing time for bus delays, driver-receiver skews and address decode the bus master sends SYNC to signal that a transfer will take place between the bus master and the addressed device. The type of cycle is identified by the state of the WTBT and the REF lines. Transfer initiation occurs when the bus master asserts DIN or DOUT. DIN and DOUT are used to control the direction of data flow. DIN causes the flow to be from slave to master (read cycle) and DOUT from master to slave (write cycle). Transfer termination is caused by the address device (slave) asserting RPLY. This indicates to the master that the read data is available on the address/data lines or that the write data has been received by the slave. In response to RPLY the bus master drops DIN or DOUT and the slave in turn drops RPLY. For a read-modify-write cycle the DIN-RPLY sequence is followed by a DOUT-RPLY sequence. This allows read-modify-write to be done with only one address assertion. The LSI-11* also has a protocol to allow for refresh of dynamic RAMs. Refresh is normally done under control of the LSI-11* microcode. A refresh cycle consists of a DIN-RPLY sequence with RFSH active. During a refresh cycle no data is transferred and only A1-A6 have any significance. These addresses are used to indicate which row of a dynamic RAM is to be refreshed. Sixty-four refresh cycles are generated in a burst every 1.6 ms.

There are several points about the bus timing that should be mentioned in passing as they will influence some of the

III

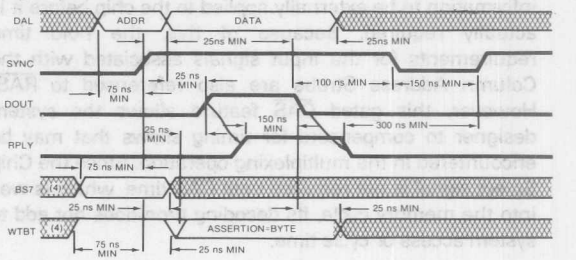
READ (REFRESH) CYCLE TIMING

Figure 1



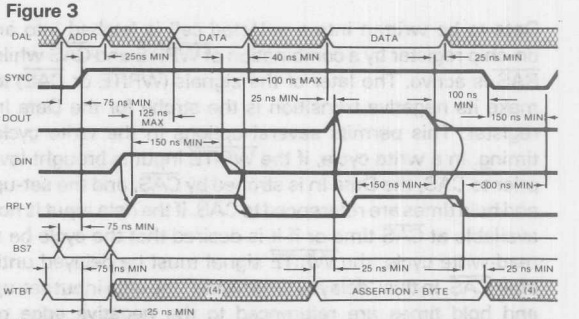
WRITE CYCLE TIMING

Figure 2



READ MODIFY WRITE CYCLE TIMING

Figure 3



*LSI-11 is a trademark of Digital Equipment Corporation

decisions made later. Since the transfers on the bus are asynchronous the memory does not have to respond in a fixed period of time. This is unlike many other microprocessors that favor synchronous transfers. Another point that should be made is that the cycle time requirements for the memory are not very stringent. In fact, the absolute minimum cycle time with a 0 ns access memory is over 800 ns. This leaves quite a bit of 'dead' time in the cycle as far as the memory is concerned.

The final point is that logically there is no difference between transfers between the CPU and memory, or CPU and peripheral. Usually, the upper 4K words of the 32K word address space is reserved for peripheral addresses. When an address within the range is placed on the bus, BS7 is asserted to flag the address as being within the 4K I/O page. There is, however, no reason why the memory cannot be made to respond to some of the addresses in the I/O page as long as it does not conflict with peripheral addresses.

MK4027 FUNCTIONAL DESCRIPTION

Addressing

The 12 address bits required to decode 1 of the 4096 cell locations within the MK4027 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. The internal circuitry of the MK4027 is designed to allow the column information to be externally applied to the chip before it is actually required. Because of this, the hold time requirements for the input signals associated with the Column Address Strobe are also referenced to $\overline{RAS}$. However, this gated $\overline{CAS}$ feature allows the system designer to compensate for timing skews that may be encountered in the multiplexing operation. Since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle, its decoding time does not add to system access or cycle time.

Data Input/Output

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the data input is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

Data Output Latch

Any change in the condition of the Data Out Latch is initiated by the $\overline{CAS}$ signal. The output buffer is not affected by memory (refresh) cycles in which only the $\overline{RAS}$ signal is applied to the MK4027. Whenever $\overline{CAS}$ makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then at access time the output latch and buffer will contain the input data. Once having gone active, the output will remain valid until the MK4027 receives the next $\overline{CAS}$ negative edge. Intervening refresh cycles in which a $\overline{RAS}$ is received (but no $\overline{CAS}$) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK4027 receives a $\overline{CAS}$ but no $\overline{RAS}$ signal (regardless of the state of any other inputs). The output will also assume the open circuit state in normal cycles (in which both $\overline{RAS}$ and $\overline{CAS}$ signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The output resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135 Ω typically. The output resistance to V_{SS} (logic 0 state) is 125 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK4027 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

Refresh

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a $\overline{RAS}$ signal occurs, accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select ($\overline{CS}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the

selected cell. If, during a refresh cycle, the MK4027 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. However, if "$\overline{RAS}$-only" refresh cycles (where $\overline{RAS}$ is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open circuit. The output buffer will regain activity with the first cycle in which a $\overline{CAS}$ signal is applied to the chip.

Power Dissipation/Standby Mode

Most of the circuitry in the MK4027 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operation frequency rather than active duty cycle. Typically, the power is 170 mW at 1 μsec cycle rate for the MK4027 with a worse case power of less than 470 mW at 320 nsec cycle time. To minimize the overall system power, the Row Address Strobe ($\overline{RAS}$) should be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a $\overline{RAS}$, however will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the outputs. If the $\overline{RAS}$ signal is decoded and supplied only to the selected chps, then the Chip Select ($\overline{CS}$) input of all chips can be at a logic 0.

The chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the $\overline{CS}$ input of all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-OR'd" outputs from turning on with opposing force. Note that the MK4027 will dissipate considerably less power when the refresh operation is accomplished with a "$\overline{RAS}$-only" cycle as opposed to a normal $\overline{RAS}/\overline{CAS}$ memory cycle.

Page Mode Operation

The "page Mode" feature of the MK4027 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and keeping the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common.

This "page mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. The chip select input ($\overline{CS}$) is operative in page mode cycles just as in normal cycles. It is not necessary that the chip be selected during the first operation in a sequence of page cycles. Likewise, the $\overline{CS}$ input can be used to select or disable any cycle(s) in a series of page cycles. This feature allows the page boundry to be extended beyond the 64 column locations in a single chip. The page boundary can be extended by applying $\overline{RAS}$ to multiple 4K memory blocks and decoding $\overline{CS}$ to select the proper block.

MK4116 FUNCTIONAL DESCRIPTION

Addressing

The 14 address bits required to decode 1 of the 16,384 cell locations within the MK4116 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time Specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row Address to Column address information.

Note that $\overline{CAS}$ can be activated at any other time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK4116 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

Data Input/Output

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (Din) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the Din is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, Din is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows Din referenced to $\overline{CAS}$).

Data read from the selected cell will be available at the output within the specified access time.

Data Output Control

The normal condition of the Data Output (Dout) of the MK4116 is the high impedance (open-circuit) state. That is to say, anytime $\overline{CAS}$ is at a high level, the Dout pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. Dout will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

If the memory cycle in progrss is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until $\overline{CAS}$ is taken to the precharge (logic 1) state, whether or not $\overline{RAS}$ goes into precharge.

If the cycle in progress is an "early-write" cycle ($\overline{WRITE}$ active before $\overline{CAS}$ goes active), then the output pin will maintain the high impedance state through the entire cycle. Note that with this type of output configuration, the user is given full control of the Dout pin simply by controlling the placement of $\overline{WRITE}$ command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle.)

This type of output operation results in some very significant system implications.

Common I/O Operation - If all write operations are handled in the "early write" mode, then Din can be connected directly to Dout for a common I/O data bus.

Data Output Control

Dout will remain valid during a read cycle from tCAC until $\overline{CAS}$ goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This also makes the $\overline{RAS}/\overline{CAS}$ clock timing relationship very flexible.

Methods of Chip Selection

Since Dout is not latched on the 4116, $\overline{CAS}$ is not required to turn off the outputs of unselected memory devices in a matrix. This means both $\overline{CAS}$ and/or $\overline{RAS}$ can be decoded for chip selection. That is, only the devices that receive both $\overline{RAS}$ and $\overline{CAS}$ will perform normal memory cycles. Those that receive $\overline{RAS}$ only will perform a refresh cycle; those devices selected are active. The remainder of the memory array is in standby. The disadvantage of this method is that the $\overline{RAS}$ decoder time usually extends the system access time. If $\overline{CAS}$ decode is used, the decode time may be hidden in the tRCD multiplexing window and thereby does not increase the system access time. The disadvantage of this method is that all unselected devices are active and performing $\overline{RAS}$-only refresh cycles. If both $\overline{RAS}$ and $\overline{CAS}$ are decoded, then a two-dimensional (X, Y) chip select array may be realized.

Output Interface Characteristics

The three state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135 Ω typically. The resistance to V_{SS} (logic 0 state) is 95 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK4116 refresh operation. This allows all system logic except the RAS timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

Page Mode Operation

The "Page Mode" feature of the MK4116 allows for succesive memory operations at multiple column locations of the same row addrss with increase speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

During a page mode operation, any combination of read, write, or read/modify/write cycles may be performed to any sequence of addresses within the selected row.

The page boundary of the MK4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. Note that the maximum number of cycles within a page mode is bounded by the maximum $\overline{RAS}$ active time. However, in system applications which utilize more than 16,384 data words, (more than one 16K memory block), the page boundary can be extended by using $\overline{CAS}$ rather than $\overline{RAS}$ as the chip select signal. $\overline{RAS}$ applied to all devices to latch the row address into each device and then $\overline{CAS}$ is decoded and serves as a page cycle select signal. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ signals will execute a read or write cycle.

performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction is power is reflected in the I_{DD3} specification called out in the MK4116 data sheet.

Power Considerations

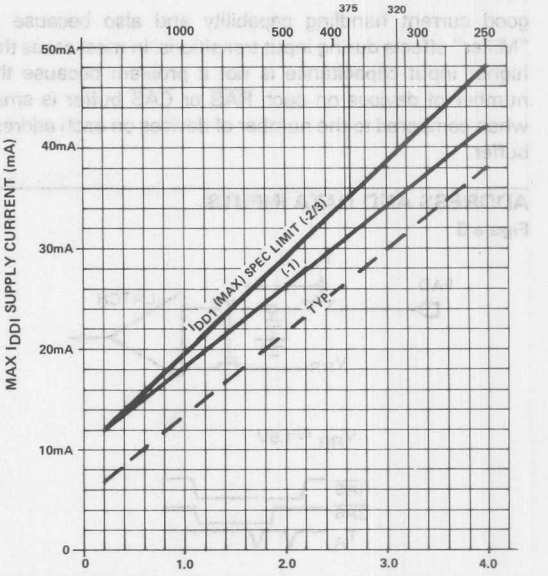
Most of the circuitry used in the MK4116 is dynamic and most of the power drawn is the result of an address strobe edge. Consequently the dynamic power is primarily a function of operating frequency rather than active duty cycle. This current characteristic of the MK4116 precludes inadvertant burn out of the device in the event that the clock inputs become shorted to ground due to system malfunction.

Although no particular power supply noise restriction exists other than the supply voltages remain within the specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the device. This insures optimum system performance and reliability. Bulk capacitance requirements are minimal since the MK4116 draws very little steady state (DC) current.

In systems applications requiring lower power dissipation, the operating frequency (cycle rate) of the MK4116 can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the I_{DD1} (max) spec limit curve illustrated in Figure 4. NOTE: The MK4116 family is guaranteed to have a I_{DD1} requirement of 35 mA @ 375 ns cycle with an ambient temperature range from 0° to 70°C. A lower operating frequency, for example 1 microsecond cycle, results in a reduced maximum I_{DD1} requirement of under 20 mA with an ambient temperature range from 0° to 70°C.

It is possible to operate certain versions of the MK4116 familty (the -2 and -3 speed selections for example) at frequencies higher than 2.66 MHz (375 ns cycle), provided all AC operating parameters are met. Operation at shorter cycle times (<375 ns) results in a higher power dissipation and, therefore, a reduction in ambient temperature is required.

Although $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the MK4116, overall system power is minimized if the Row Address Strobe ($\overline{RAS}$) is used for this purpose. All unselected devices (those which do not receive a $\overline{RAS}$) will remain in a low power (standby) mode regardless of the state of $\overline{CAS}$.



CYCLE RATE (MHz)=$10^3/t_{RC}$ (ns)

Maximum I_{DD1} versus cycle rate for device operation at extended frequencies. I_{DD1} (max) curve is defined by the equation.

I_{DD1} (max) mA = 10 + 9.4 x cycle rate (MHz) for -2/3 only
I_{DD1} (max) mA = 10 + 8.0 x cycle rate (MHz) for -1 only

TERMINAL CHARACTERISTICS OF THE MK4027 AND MK4116

Inputs

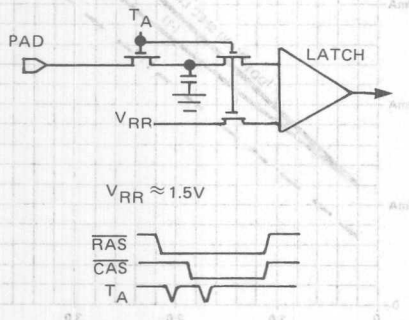
Addresses, Chip Seclect and Din - The address, Din and CS input circuit for the MK4027 and MK4116 is shown in Fig. 5. This particular input curcuit has some characteristics that make it particularly useful for the address and data inputs. First of all, it has a low input capacitance which is very important in large arrays of memory chips where it is desirable to tie many addresses inputs together and to drive them with a single buffer. This circuit also allows the address hold time for row adress to be very short. This makes the available 'window' for address multiplexing as wide as possible.

Clocks - The $\overline{RAS}$, $\overline{CAS}$, and $\overline{WRITE}$ inputs are basically MOS inverter stages. (Fig 6) The $\overline{RAS}$ input buffer is always active (the depletion load on the inverter is always supplying current to the inverter) because the device must always be able to respond to $\overline{RAS}$ transitions. The $\overline{RAS}$ input buffer accounts for the vast majority of the 1.5 ma of standby current on V_{DD}. The $\overline{CAS}$ and $\overline{WRITE}$ buffers differ from the $\overline{RAS}$ buffer in that the load device is clocked. When the memory is in standby ($\overline{RAS}$ high), the $\overline{CAS}$ and $\overline{WRITE}$ buffers load device is turned off. The input capacitance of

the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WRITE}$ buffers is fairly high (10pf) in comparison to the address inputs. This is because the input transistors are comparatively large since they have to have good current handling capability and also because of "Miller" effects during input transitions. In most cases this higher input capacitance is not a problem because the number of devices on each $\overline{RAS}$ or $\overline{CAS}$ buffer is small when compared to the number of devices on each address buffer.

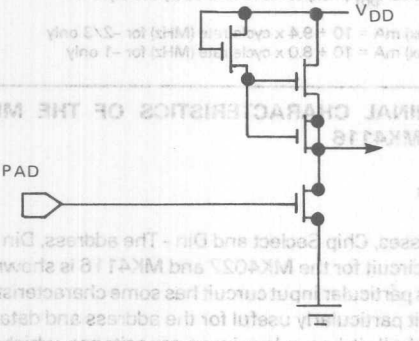
ADDRESS AND DATA INPUTS

Figure 5



CLOCK INPUT CIRCUIT

Figure 6



MK4116 AND MK4027 COMPATIBLE DESIGNS

Because of their similarities it is very easy to design a memory system that will accommodate either the MK4027 or the MK4116. This is often a very desirable goal because it allows the memory system to be tailored to meet a wide range of overall system requirements. There are some differences, however, between the MK4027 and MK4116 that require special consideration.

Refresh and Dout Interaction

In many systems that use transparent refresh, such as this *LSI-11 memory system, it is required that refresh take place immediately after a memory read or write cycle. If refresh takes place after a read cycle it may be required that the read data be held while refresh takes place. The only way to accomplish this in a compatible design is by adding data latches. The MK4027 will, in fact, work without latches if "$\overline{RAS}$ only" refresh is used. The MK4116, however, requires that $\overline{CAS}$ be held low to maintain the output data which means that no cycle may start while the data is being held.

Address Multiplexing

The differing address requirements for the MK4027 and MK4116 can be accommodated without jumpers. Fig. 7 shows a multiplexing scheme that uses the 'extra' multiplexer in a 74S158 to supply an inverted address to half the memory. When row addreses are selected two of the multiplexor outputs contain the same address data. The MK4027 will ignore this address data because it is applied to the $\overline{CS}$ input which is a 'don't care' at $\overline{RAS}$ time. The MK4116, however, sees this input as another address and will strobe it in at $\overline{RAS}$ time. When column addresses are selected the extra multiplexor contains a complement address. The MK4027 uses this input as a $\overline{CS}$ input and the MK4116 uses it as another column address. Two high order addresses are used such that they are part of the $\overline{RAS}$ decode for the MK4027 but are not terms in the $\overline{RAS}$ decode for the MK4116. The net effect is that for the MK4027 half the chips will receive $\overline{CS}$ and only one selected row will receive $\overline{RAS}$. For the MK4116 the column data on half the rows will be reversed around A6.

Generating The Memory Timing

The timing generator for the *LSI-11 memory system has many responsibilities. It must provide the row address hold time (t_{RAH}), it must generate the multiplexing control signal, it must provide column address setup time, it must generate a column address strobe delay, it must generate a valid data or end of write signal, and must provide the necessary precharge interval (t_{RP}).

Any number of methods may be used to generate this timing such as an oscillator driving a counter or a shift register; or a series of one-shots. However, each of these methods has a number of problems. The oscillator is necessarily asynchronous to cycle initiation and the cycle startup problems are acute. The one-shot approach simply cannot be made accurate when short delays are required. The simplest and most reliable solution to generating the necessary timing edges is to use a delay line.

The timing and control logic is shown in Fig. 8. All cycle timing is derived from the delay line. The input to the delay line is a low going signal that propagates to the end of the line and resets the input such that the new memory cycle can be initiated whenever the output of the line returns high.

The delay line shown has a 200 ns total delay with 5 taps at 40 ns intervals. This line was chosen because it was a standard 'off the shelf' item and was adequate for prototyping. The delay line timing and resulting system timing for read and write cycles is shown in Figs. 9 and 10.

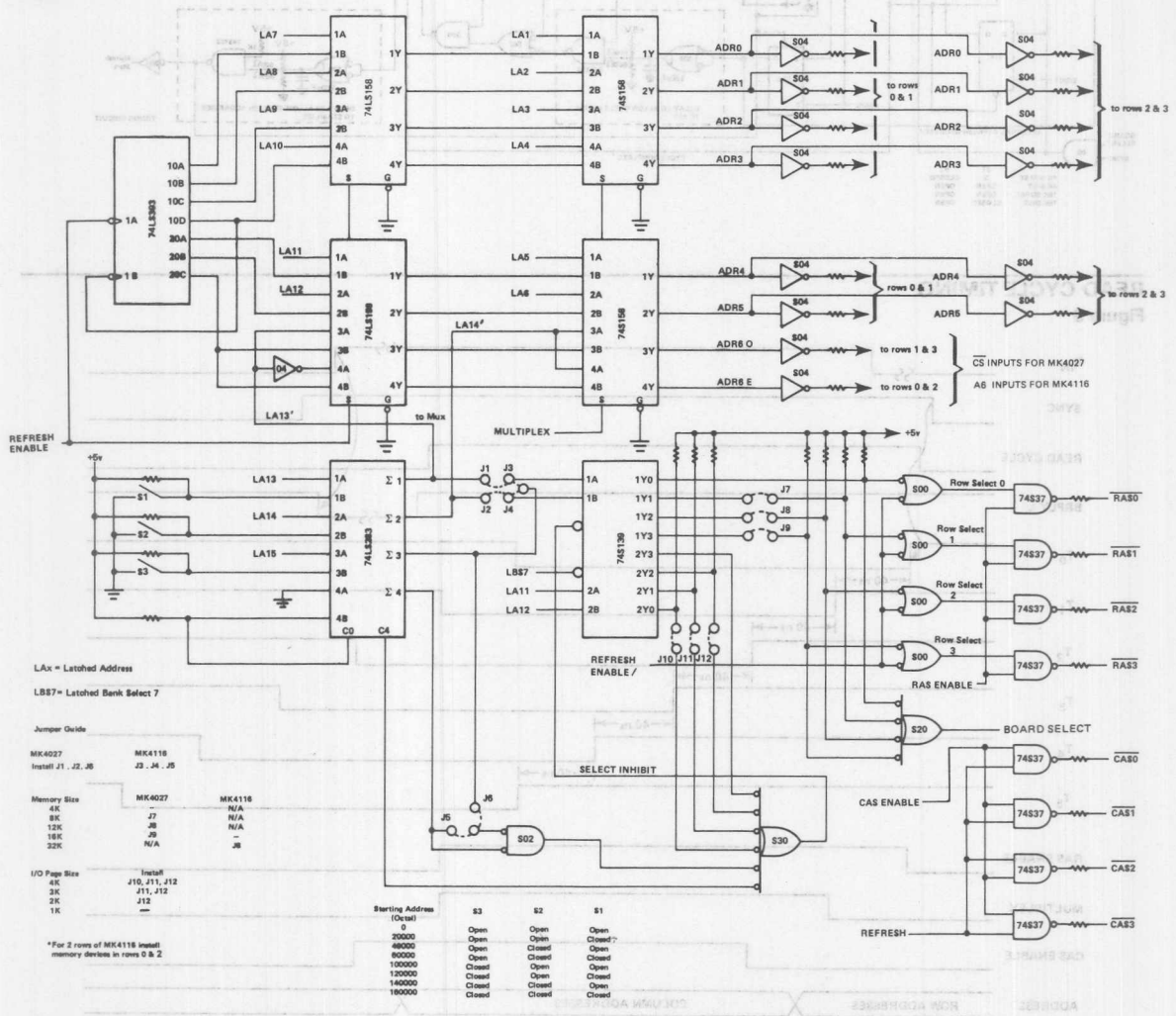
The synchronous refresh timing is similar to the read cycle timing but the asynchronous refresh (Fig. 11) cycle has some interesting features. When the refresh interval timer indicates that a refresh should occur all further external cycles are inhibited from starting. After 50 ns delay if no cycle is in progress the address multiplexor can be switched to select the refresh addresses from the refresh address counter. After an additional 50 ns delay to allow refresh addresses to stabilize, the cycle is started and proceeds much like any other cycle except no RPLY is generated and $\overline{CAS}$ is inhibited.

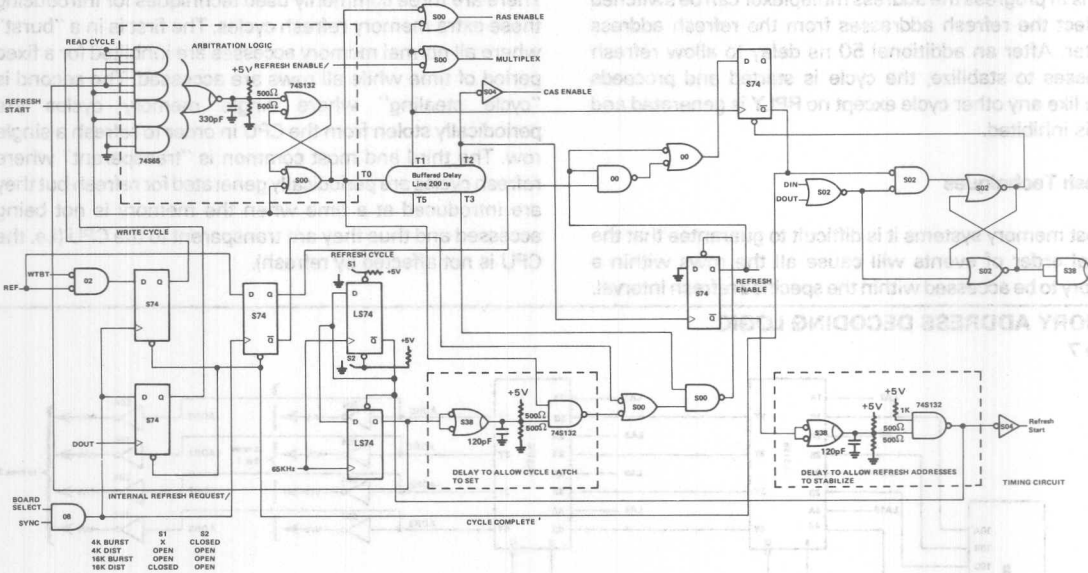
Refresh Techniques

In most memory systems it is difficult to guarantee that the normal order of events will cause all the rows within a memory to be accessed within the specified refresh interval. For this reason, most dynamic memory systems have special circuitry that will cause extra memory cycles in an ordered manner such that all rows of memory devices are accessed within the 2 ms interval.

There are three commonly used techniques for introducing these extra memory refresh cycles. The first is in a "burst" where all normal memory accesses are inhbiited for a fixed period of time while all rows are accessed. The second is "cycle stealing" where single memory cycles are periodically stolen from the CPU in order to refresh a single row. The third and most common is "transparent" where refresh cycles are periodically generated for refresh but they are introduced at a time when the memory is not being accessed and thus they are transparent to the CPU (i.e. the CPU is not affected by refresh).

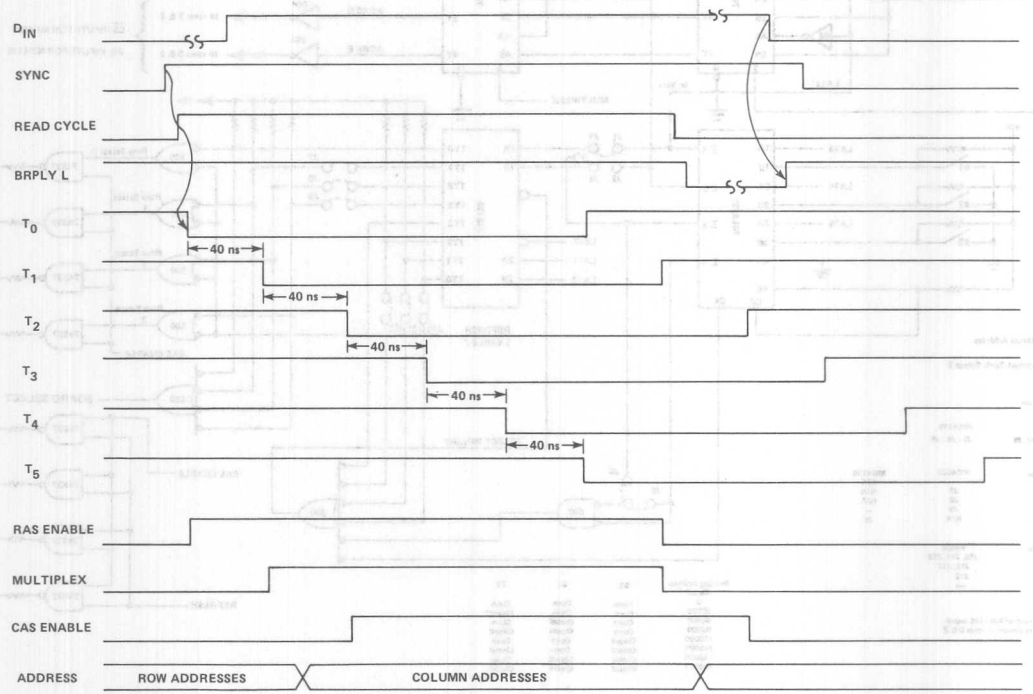
MEMORY ADDRESS DECODING LOGIC
Figure 7

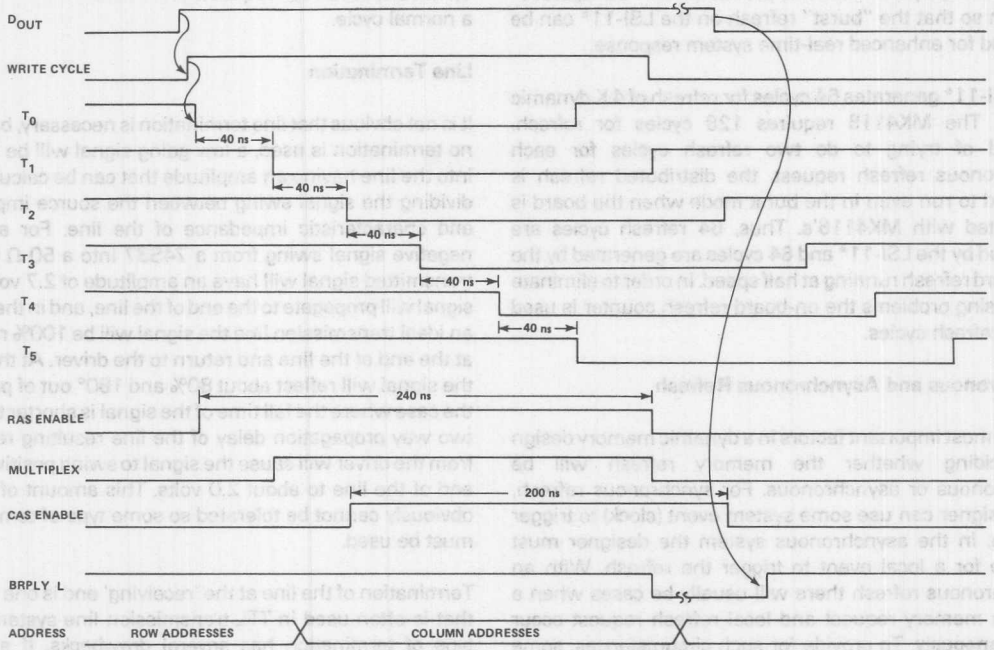




READ CYCLE TIMING

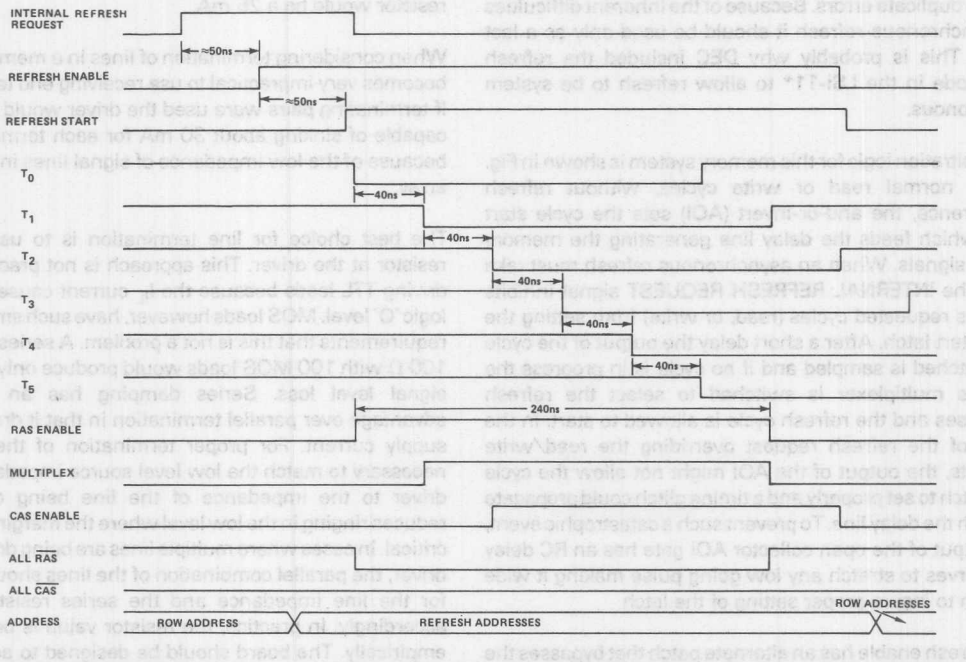
Figure 9





INTERNAL REFRESH CYCLE TIMING

Figure 11



The *LSI-11 microcode has provisions for performing "burst" refresh and the memory system described here will respond to the "burst" refresh from the LSI-11*. In addition, this memory system also has provisions for "transparent" refresh so that the "burst" refresh on the LSI-11* can be disabled for enhanced real-time system response.

The LSI-11* generates 64 cycles for refresh of 4 K dynamic RAMs. The MK4116 requires 128 cycles for refresh. Instead of trying to do two refresh cycles for each synchronous refresh request, the distributed refresh is allowed to run even in the burst mode when the board is populated with MK4116's. Thus, 64 refresh cycles are provided by the LSI-11* and 64 cycles are generated by the on-board refresh running at half speed. In order to eliminate addressing problems the on-board refresh counter is used for all refresh cycles.

Synchronous and Asynchronous Refresh

One of most important factors in a dynamic memory design is deciding whether the memory refresh will be synchronous or asynchronous. For synchronous refresh, the designer can use some system event (clock) to trigger refresh. In the asynchronous system the designer must provide for a local event to trigger the refresh. With an asynchronous refresh there will usually be cases when a system memory request and local refresh request occur simultaneously. To provide for such circumstances, some arbitration scheme must be present on the asyhchronously refreshed memory. Extreme care must be taken in the design of the arbitration logic because if it does not contain adequate safeguards the memory system can (and will) malfunction causing some rather interesting and impossible to duplicate errors. Because of the inherent difficulties of asynchronous refresh it should be used only as a last resort. This is probably why DEC included the refresh microcode in the LSI-11* to allow refresh to be system synchronous.

The arbitration logic for this memory system is shown in Fig. 8. For normal read or write cycles, without refresh interference, the and-or-invert (AOI) sets the cycle start latch which feeds the delay line generating the memory timing signals. When an asynchronous refresh must take place the INTERNAL REFRESH REQUEST signal inhibits any bus requested cycles (read, or write) from setting the cycle start latch. After a short delay the output of the cycle start latched is sampled and if no cycle is in progress the address multiplexer is switched to select the refresh addresses and the refresh cycle is allowed to start. In the event of the refresh request overriding the read/write requests, the output of the AOI might not allow the cycle start latch to set properly and a timing glitch could propagate through the delay line. To prevent such a catastrophic event, the output of the open collector AOI gate has an RC delay that serves to stretch any low going pulse making it wide enough to insure proper setting of the latch.

The refresh enable has an alternate patch that bypasses the arbitration delay. This is used for synchronous refresh cycles that are generated by the LSI-11*. The arbitration can be bypassed because it is possible to merge the synchronous refresh requests and not cause a conflict with a normal cycle.

Line Termination

It is not obvious that line termination is necessary, but it is. If no termination is used, a low going signal will be injected into the line having an amplitude that can be calculated by dividing the signal swing between the source impedance and characteristic impedance of the line. For a 3 Volt negative signal swing from a 74S37 into a 50 Ω line the transmitted signal will have an amplitude of 2.7 volts. This signal will propagate to the end of the line, and in the case of an ideal transmission line the signal will be 100% reflected at the end of the line and return to the driver. At the driver the signal will reflect about 80% and 180° out of phase. In the case where the fall time of the signal is shorter than the two way propagation delay of the line resulting reflection from the driver will cause the signal to swing positive at the end of the line to about 2.0 volts. This amount of ringing obviously cannot be tolerated so some type of termination must be used.

Termination of the line at the 'receiving' end is one method that is often used in TTL transmission line systems. This type of termination has several drawbacks. If a simple pullup resistor to +5 volts is used, the low level DC current through a resistor with a resistance equal to the impedance of the line will in most cases consume almost all of the drive capability of the bus driver. Even if the line impedance is as high as 200 Ω the logic 'O' level current through a 200 Ω resistor would be a 25 mA.

When considering termination of lines in a memory array it becomes very impractical to use receiving end termination. If terminating pairs were used the driver would have to be capable of sinking about 30 mA for each terminated line because of the low impedance of signal lines in a memory array.

The best choice for line termination is to use a series resistor at the driver. This approach is not practical when driving TTL loads because the I_{IL} current causes a loss of logic 'O' level. MOS loads however, have such small current requirements that this is not a problem. A series resistor of 100 Ω with 100 MOS loads would produce only 0.1 volt of signal level loss. Series damping has an additional advantage over parallel termination in that it draws no DC supply current. For proper termination of the line it is necessary to match the low level source impedance of the driver to the impedance of the line being driven.This reduces ringing in the low level where the margins are most critical. In cases where multiple lines are being driven by the driver, the parallel combination of the lines should be used for the line impedance and the series resistor chosen accordingly. In practice, the resistor value is best chosen empirically. The board should be designed to accomodate

the resistors and then different values tried on a prototype. The waveform with the ideal resistor will be slightly underamped.

DELAY TIME CALCULATIONS

The switching delays for TTL devices driving capacitive loads such as memory signal lines can be appropriated by using the equation for the charge time of a lumped constant RC circuit. R will be the maximum output impedance of the gate plus the series damping resistance, and C is the sum of the capacitances of the inputs being driven plus the capacitance of the board. When calculating the capacitance of the line the data sheet typical values for capacitance should be used rather than the maximums. This is because high input capacitance is not a function of the wafer lot, and the probability of having mostly worst case capacitance on the same signal line is very very small.

The equation for the maximum rise time is:

$$t_r = -RC \ln \frac{3.85\ V - V_{IH}}{3.85\ V - 0.2\ V} = -RC \ln \frac{3.85\ V - V_{IH}}{3.65\ V}$$

V_{IH} = 2.2 volts for addresses on 4027

V_{IN} = 2.4 volts for addresses on 4116 and clocks on 4027

V_{IH} = 2.7 volts for clocks on 4116
The fall time is:

$$t_f = -RC \ln \frac{.8}{3.95} = 1.6\ RC$$

SIGNAL	V_{IH}	DRIVER	SERIES RESISTOR	LOADS/ LINE	LOAD CAPACITANCE	t_{pLH}	t_{pHL}
4027 CLOCKS	2.4	74S37	22 Ω	16	148pF	15ns	6.5ns
4116 CLOCKS	2.7	74S37	22 Ω	16	148pF	19ns	6.5ns
4027 ADDRESSES	2.2	74S37	22 Ω	32	169pF	18ns	10ns
4116 ADDRESSES	2.4	74S04	22 Ω	32	168pF	21ns	10ns

Table 1 Calculated Propagation Delays for Memory Signal Buffers

Power Distribution and Decoupling

The layout for dynamic memories is of special importance. Layout techniques that have been used successfully in the past for older generation MOS memories are simply inadequate for current state-of-the-art memories such as the MK4027 and the MK4116. The newer devices have shallow diffusions that make possible fast memory devices but the shallow diffusions and fast switching speeds create larger current transients with high frequency components than did the older designs. (Fig. 12) In order to tame these current transients and prevent them from generating voltage spikes that can cause loss of data and 'soft' errors every effort must be made to minimize the impedance in the decoupling path for the device.

The decoupling path is the trace distance from a power pin through a decoupling capacitor and to package ground. The impedance of this path is determined by the line inductance and the series impedance of the decoupling capacitor. Because the current transients of the MK4027 and MK4116 have significant harmonic content up to 500MHz the line inductance can be minimized either by providing a power plane or by griding the power. In order to increase the effectiveness of the grided power, ceramic monolithic decoupling capacitators with good high frequency response should be placed judiciously. A capacitor placement that has shown to be very effective is shown in Fig. 13. The inductance of capacitor leads has a detrimental effect and therefore lead lengths should be kept to a minimum. V_{DD} and V_{BB} are decoupled at every other chip with 0.1 μF capacitors such that the decoupling creates a 'checkerboard' pattern. This particular pattern was used on the LSI-11* memory board and measurements of the V_{DD} noise with a differential probe showed that the noise was below 400 mV peak-to-peak.

III

FIG. 12 CURRENT WAVEFORMS FOR MK4116

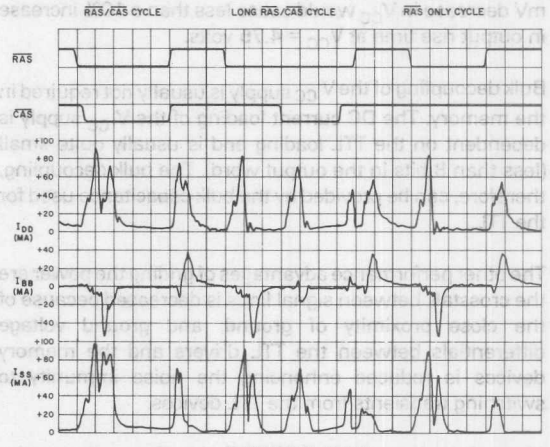
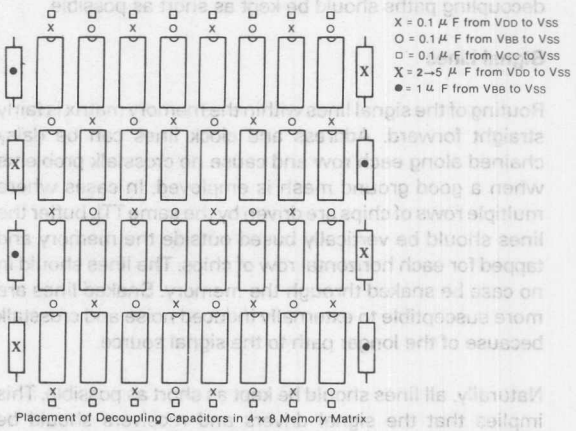


FIG. 13



Placement of Decoupling Capacitors in 4 x 8 Memory Matrix

to prevent supply droop. The long term (cycle time) current requirements of the MK4027 and MK4116 are fairly low at 35 mA max. Assuming 64 memory devices all cycling at the maximum rate of 375 ns with 120 ns of precharge only 8.4 μF of capacitance is required to keep the voltage drop below .1 volts. As with the high frequency decoupling it is good practice to distribute the bulk capacitance around the storage matrix to minimize the effects of the inductive and resistive voltage drops.

Decoupling of the V_{CC} (+5) supply is fairly non-critical. In most cases only one row of memory devices is accessed at a time. The V_{CC} supply, therefore, only needs to provide enough current to charge one Dout line for each column of memories. The V_{CC} decoupling capacitors (0.1 μF) were placed at the top and bottom of each column of memories. The V_{CC} voltage at each device was measured when a data '1' was being read. The drop in V_{CC} was less than 300 mV. Calculations of the resultant rise time indicate that a 300 mV decrease in V_{CC} would cause less than a 10% increase in output rise time at V_{CC} = 4.75 volts.

Bulk decoupling of the V_{CC} supply is usually not required in the memory. The DC current loading of the V_{CC} supply is dependent on the TTL loading and is usually quite small (less than 8 bits in the output word). The bulk decoupling, therefore, can be provided by the bulk capacitance used for the TTL.

The other performance advantages of griding the power are the crosstalk between signal lines is decreased because of the close proximity of ground; and ground voltage differentials between the TTL drivers and the memory devices is reduced enhancing the noise immunity to switching transients from the TTL devices.

Most of the layout techniques used in the memory array should be extended to the TTL circuitry on all boards. Ground should be grided wherever possible. The decoupling paths should be kept as short as possible.

Signal Lines

Routing of the signal lines within the memory matrix is fairly straight forward. Address and clock lines can be daisy chained along each row and cause no crosstalk problems when a good ground mesh is employed. In cases where multiple rows of chips are driven by the same TTL buffer the lines should be vertically bused outside the memory and tapped for each horizontal row of chips. The lines should in no case be snaked through the memory. Snaked lines are more susceptible to externally induced noise and crosstalk because of the longer path to the signal source.

Naturally, all lines should be kept as short as possible. This implies that the signal drivers and receivers should be physically close to the memory array. In cases where there are a large number of memory chips in each row the address drivers should be placed in the center of the array. (Fig. 16) If the $\overline{RAS}$ and $\overline{CAS}$ buffers drive one row of memory chips each can be placed either in the center of the array or on the side of the array. If the drivers will not fit in the middle of the matrix, they may be placed below the matrix. The signal lines would then be routed vertically and 'T'd' for each horizontal connection. In such cases, it is recommended that each stub be the same length in order to minimize the distortion of the signal edges caused by mismatched stubs.

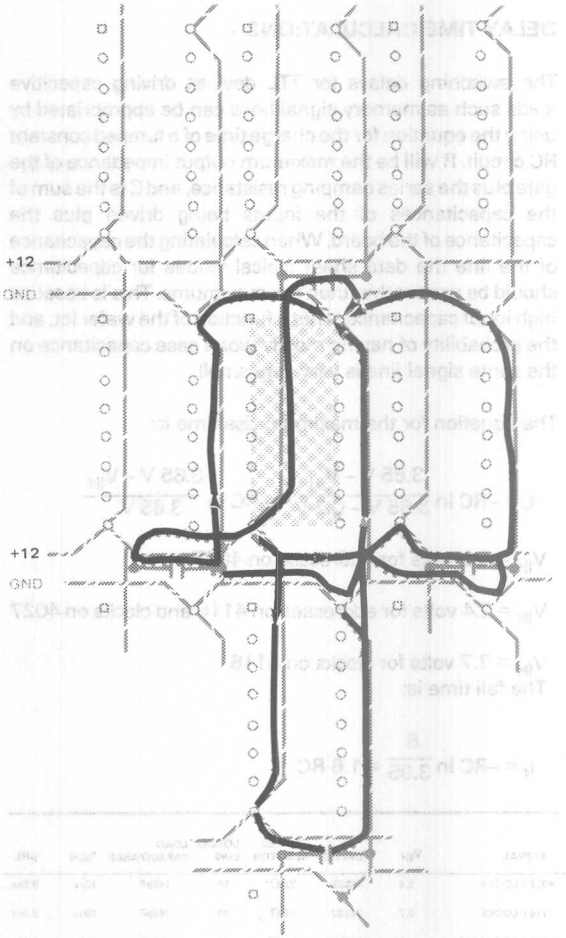


FIG. 14

Decoupling Currents With Grided Power And Checkerboard Decoupling

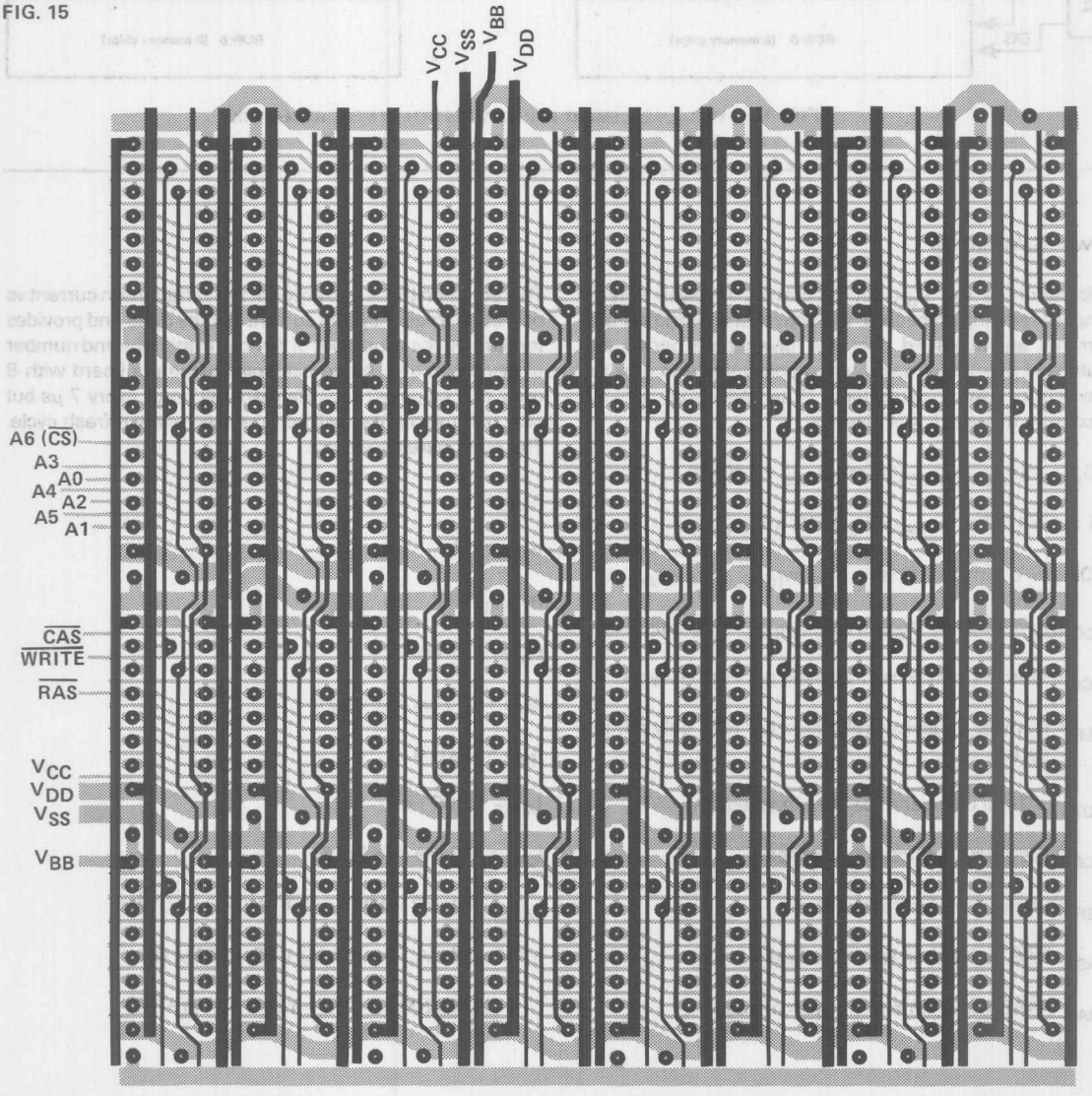
MISCELLANEOUS POWER CONSIDERATIONS

Power Sequencing

The data sheets for the MK4027 and MK4116 state that no special power sequencing is required for proper device operation. This does not mean that the power sequencing should be ignored. In many systems the power supply lines exhibit overshoot on power up. This can cause V_{DD} at the memory to exceed data sheet limits for a short period of time. If V_{BB} is not applied when V_{DD} overshoots, breakdown can occur and destroy the memory. If a system does have this overshoot, sequencing the supplies so that V_{BB} is applied first will provide extra margin and help prevent device destruction.

The data sheet specified that V_{BB} should not be allowed to go positive with respect to ANY other input. If it does, injection currents can cause loss of functionality. Special precautions should be taken in the V_{BB} power distribution to prevent this occurance. A high current Schottky diode from V_{BB} to ground can protect against many of the hazards such as an open V_{BB} supply. Note that the layout in Fig 15 has the V_{BB} run next to the ground in the memory array. This will help reduce the chance of emory damage should a screwdriver or scope probe get loose in the system.

SUGGESTED P.C. LAYOUT FOR MK4027 OR MK4116
FIG. 15



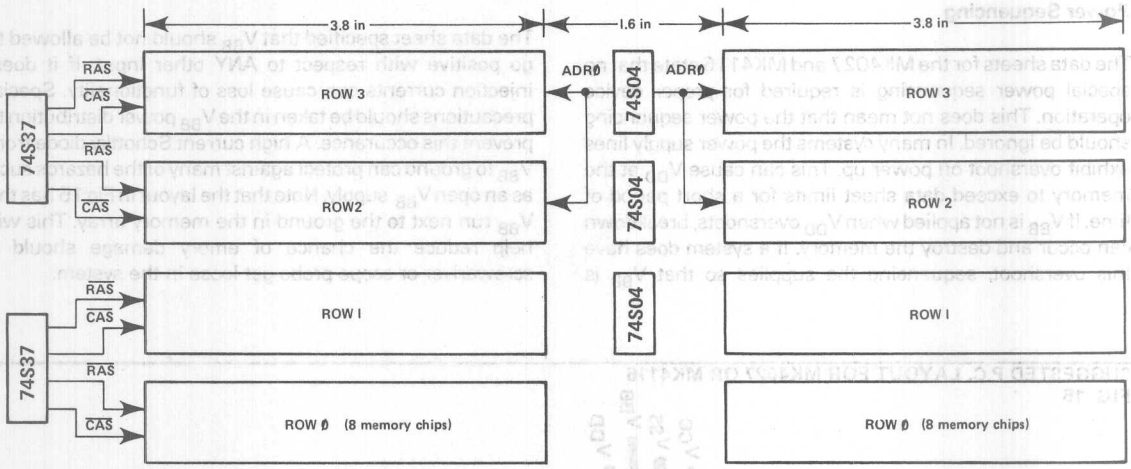


FIG. 16 TYPICAL PLACEMENT FOR DRIVERS WITHIN MEMORY MATRIX

Power Calculations

Calculation of the V_{DD} supply current involves a fairly simple averaging procedure. The active refresh and standby currents are averaged over any given time period and multiplied times the maximum supply voltage to give the maximum power dissipation. The equation for the maximum average I_{DD} is given by:

$$IDD_{AVE} = [n_{ACC} \times c_{ACC} [10\ mA\ (t_{RAS} + 120\ ns) +$$

$$9.4\ mA \times 10^{-6}\ s] + n_{REF} \times c_{REF} [\ 10\ mA\ (t_{RRAS} +$$

$$120\ ns) + 6.5\ mA \times 10^{-6} s] + I_{DD2} [n_{TOTAL} \times 1s - n_{ACC} \times$$

$$c_{ACC}(t_{RAS} + 120\ ns) - n_{REF} \times c_{REF}\ (t_{RRAS} + 120\ ns)] / 1s$$

n_{ACC} = Number of devices accessed per normal cycle

n_{REF} = Number of devices refreshed per $\overline{RAS}$ only refresh cycle

n_{TOTAL} = Total number of devices in ystem

c_{ACC} = Frequency of normal accesses

c_{REF} = Frequency of refresh cycles

t_{RAS} = $\overline{RAS}$ active time for normal cycles

t_{RRAS} = $\overline{RAS}$ active time for refresh cycles

This equation takes into account the variations in current vs operating frequency and current vs duty cycle and provides for differences in number of devices in standby and number of devices active. As an example, assume a board with 8 rows of 8 chips per row. Refresh will occur every 7 μs but only half the devices will be refreshed every refresh cycle. The other parameters are:

$n_{ACC} = 8$

$n_{REF} = 32$

$n_{TOTAL} = 64$

$c_{ACC} = 2$ MHz

$c_{REF} = 1/7\ \mu s \sim 143$ kHz

$t_{RAS} = 240$ ns

$t_{RRAS} = 200$ ns

$I_{DD2} = 1.5$ ma (MK4116)

$$I_{DD_{AVE}} = 8 \times 2 \times 10^{6} [1 \times 10^{-2} A\ (240 \times 10^{-9} s)$$

$$+ 9.4 \times 10^{-3} A \times 1 \times 10^{-6} s] + 32 \times 143 \times 10^{3}$$

$$[1 \times 10^{-2} A\ (200 \times 10^{-9} s + 120 \times 10^{-9} s) + 6.5$$

$x\ 10^{-3} \times 1 \times 10^{-6}s] + 1.5 \times 10^{-3}\ [64 \times Is - 8$

$x\ 2 \times 10^{6}\ (240 \times 10^{-9}s + 120 \times 10^{-9}s) - 32 \times 143$

$x\ 10^{3}\ (20 \times 10^{-9}s + 120 \times 10(-9s)]$

$I_{DD_{AVE}} = 337.6$ ma

Power calculations for the LSI—11 board using distributed refresh and with MK4027 gives:

$n_{ACC} = 16$

$n_{REF} = 16, 32, 48, 64$

$n_{TOTAL} = 16, 32, 48, 64$

$c_{ACC} = 1$ MHz (bus limit)

$c_{REF} = 32.5$ kHz

$t_{RAS} = 240$ ns

$t_{RRAS} = 240$ ns

$I_{DD2} = 2.0$ ma

Yielding a maximum I_{DD} current of 233 mA for 4 K words, 270 mA for 8 K, 307 mA for 12 K and 344 mA for 16 K.

Using the MK4116 we have:

$n_{ACC} = 16$

$n_{REF} = 16, 32$

$n_{TOTAL} = 16, 32$

$c_{ACC} = 1$ MHz

$c_{REF} = 65$ kHz

$t_{RAS} = 240$ ns

$t_{RRAS} = 240$ ns

$I_{DD2} = 1.5$ ma

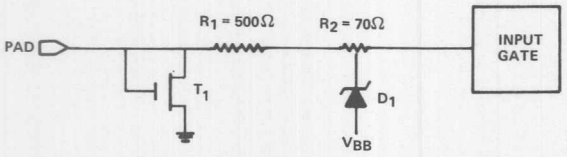
This gives a maximum average I_{DD} current of 223 mA for 16 K and 236 mA for 32 K.

It is interesting to note that on a per chip basis the Mk4116 actually consumes less power than the MK4027 even though the MK4116 is refreshed at twice the rate.

INPUT PROTECTION CIRCUIT

All signal inputs to the MK 4116 have the input protection circuit shown in Figure 1 integrated onto the chip. The purpose of the circuit is to protect the device from damage caused by static voltages that may be encountered during shipping and handling.

INPUT PROTECTIVE CIRCUITRY
Figure 1



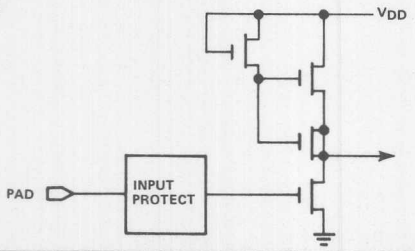
T_1 is a metal gate field transistor having a threshold voltage of approximately 12 volts, and D_1 is a N^+ –P diode whose breakdown is lowered by the presence of a gate electrode at substrate (V_{BB}) potential on the periphery of the diode.

Conventional testing of the electrostatic protection devices using a 50–100 picofarad capacitor charged to some variable potential in the range of 500 to 1000 volts and discharged into the input through a 1K-2K ohm resistor have been performed by MOSTEK and demonstrate that the protection is adequate. Customer tests of the protective devices should be limited to 50 picofarads, 500 volts discharged through a 1K ohm resistor. Exposure to conditions exceeding these may affect reliability of the device.

All power supply inputs (V_{DD}, V_{CC}, V_{SS}) are essentially large area N^+ diffusions to the P-type substrate (V_{BB}).

The functional circuitry for the clock inputs ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$) looks like:

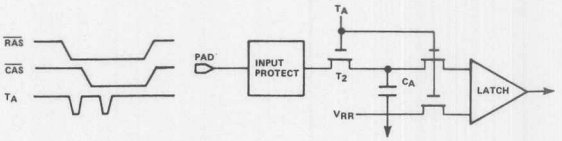
CLOCK INPUT CIRCUIT
Figure 2



which is a fairly conventional MOS inverter. When determining the input capacitance of any such circuit, the power supplies should be at normal operational levels and, if an AC signal is supplied at the input, the amplitude of this signal should be normal (0–3 volts) to reduce the voltage gain and therefore the Miller capacitance of the input stage.

The input stage for address and data input signals is:

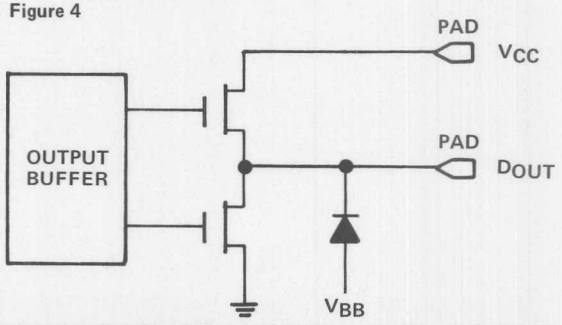
ADDRESS AND DATA INPUTS
Figure 3



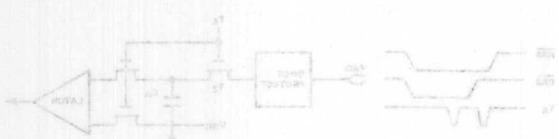
where T_A is an internally generated clock and V_{RR} an internally generated reference voltage (approximately one-eighth of V_{DD}). T_A isolates the storage capacitor C_A from the external signal as soon as possible after $\overline{RAS}$ or $\overline{CAS}$, allowing the applied signal to change during the operation of the internal latch. Note that, if the external signal switches to a level more than one threshold voltage below ground (or has negative undershoot going more than one threshold below ground) the transistor T_2 may turn back on at the improper moment, allowing the discharge of capacitor C_A and resulting in improper operation of the input latch. This is the reason that the V_{IL} of all signals is limited to –1.0 volts in the negative direction.

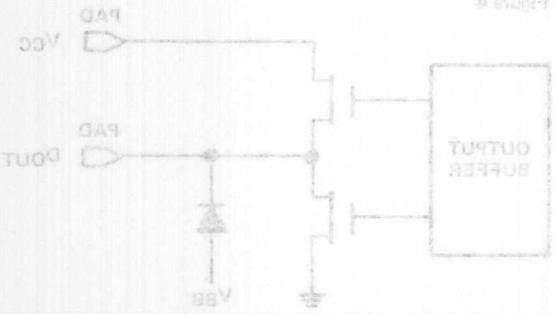
The data output circuitry is given in Figure 4.

DATA OUTPUT CIRCUITRY
Figure 4



In general, extreme care must be exercised when making measurements on the D_{OUT} that both the transistors of the output stage are turned "OFF". It is sufficient on the MK 4116 (although not on the earlier MK 4027 which has a latched output) to have V_{DD} and V_{BB} within the normal operating range and the $\overline{CAS}$ level above V_{IH} level. Under these conditions, both transistors will be held "OFF" and leakage measurements may be made on the output pin.





ADDRESSING CONSIDERATIONS WHEN TESTING THE MK4116

Testing

Customer engineers responsible for evaluation and incoming testing of Random Access Memories normally require a description of the internal topology of a device in order to check for "worst case" patterns or to optimize test sequences. This paper will provide such information for the MK4116 16-kilobit dynamic RAM.

Due to the complexity of the part, this information is not quite so straightforward as in earlier RAMs produced by Mostek. It is necessary that the test engineer keep in mind three separate topological alterations:

1. Decode Topology

   Efficient layout of the row and column decoders results in a scramble of the address inputs which must be observed if, for example, it is required that rows and columns be accessed in a "nearest neighbor" manner. The logic necessary to descramble this decode topology is given in Figure 1. Note carefully that Figure 1 gives addresses in terms of their row (R_n) and column (C_n) components. The multiplexing of R_n and C_n such that R_n is valid at RAS time and C_n is valid at CAS time produces the address input A_n. In many cases it is desirable to perform the address transformation via some software mapping technique rather than hard-wired gates. When using a software descramble, it is more convenient to have the address transformation presented in a numerical format. The address transformations are provided in a numerical form in Tables 1 and 2; Table 1 describes the row address transformation and Table 2 provides the column address transformation.

2. Data Polarity

   Utilization of a balanced sense amp located between rows 63_{10} and 64_{10} of the matrix requires that one of the two halves of the matrix invert data (this inversion is comprehended by internal circuitry so that it is transparent to the user). If it is necessary, for example, to write all 16 kilobits to a charged state, the data polarity of Figure 2 must be observed.

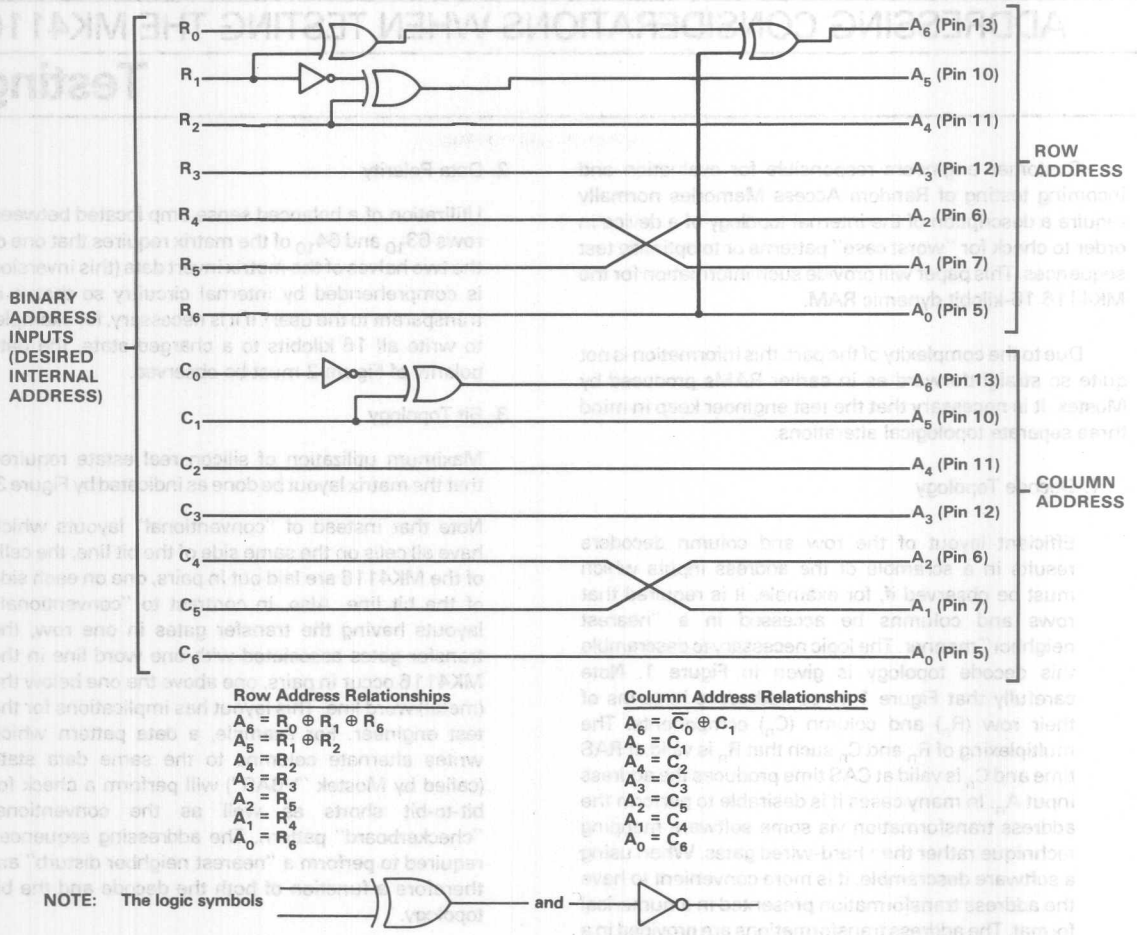
3. Bit Topology

   Maximum utilization of silicon real estate required that the matrix layout be done as indicated by Figure 3.

   Note that instead of "conventional" layouts which have all cells on the same side of the bit line, the cells of the MK4116 are laid out in pairs, one on each side of the bit line. Also, in contrast to "conventional" layouts having the transfer gates in one row, the transfer gates associated with one word line in the MK4116 occur in pairs, one above the one below the (metal) word line. This layout has implications for the test engineer. For example, a data pattern which writes alternate columns to the same data state (called by Mostek "VBAR") will perform a check for bit-to-bit shorts as well as the conventional "checkerboard" pattern. The addressing sequences required to perform a "nearest neighbor disturb" are therefore a function of both the decode and the bit topology.

   For the sake of completeness, although not strictly necessary, Figure 4 relates the location of inputs and the individual bits to the actual chip.

Figure 1



Row Address Relationships

$A_6 = R_0 \oplus R_1 \oplus R_6$
$A_5 = \overline{R_1} \oplus R_2$
$A_4 = R_2$
$A_3 = R_3$
$A_2 = R_5$
$A_1 = R_4$
$A_0 = R_6$

Column Address Relationships

$A_6 = \overline{C_0} \oplus C_1$
$A_5 = C_1$
$A_4 = C_2$
$A_3 = C_3$
$A_2 = C_5$
$A_1 = C_4$
$A_0 = C_6$

NOTE: The logic symbols and

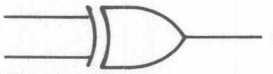
are used solely to indicate the logic function "Exclusive — OR" and "NOT", respectively; the above figure is not a suggested implementation of logic.

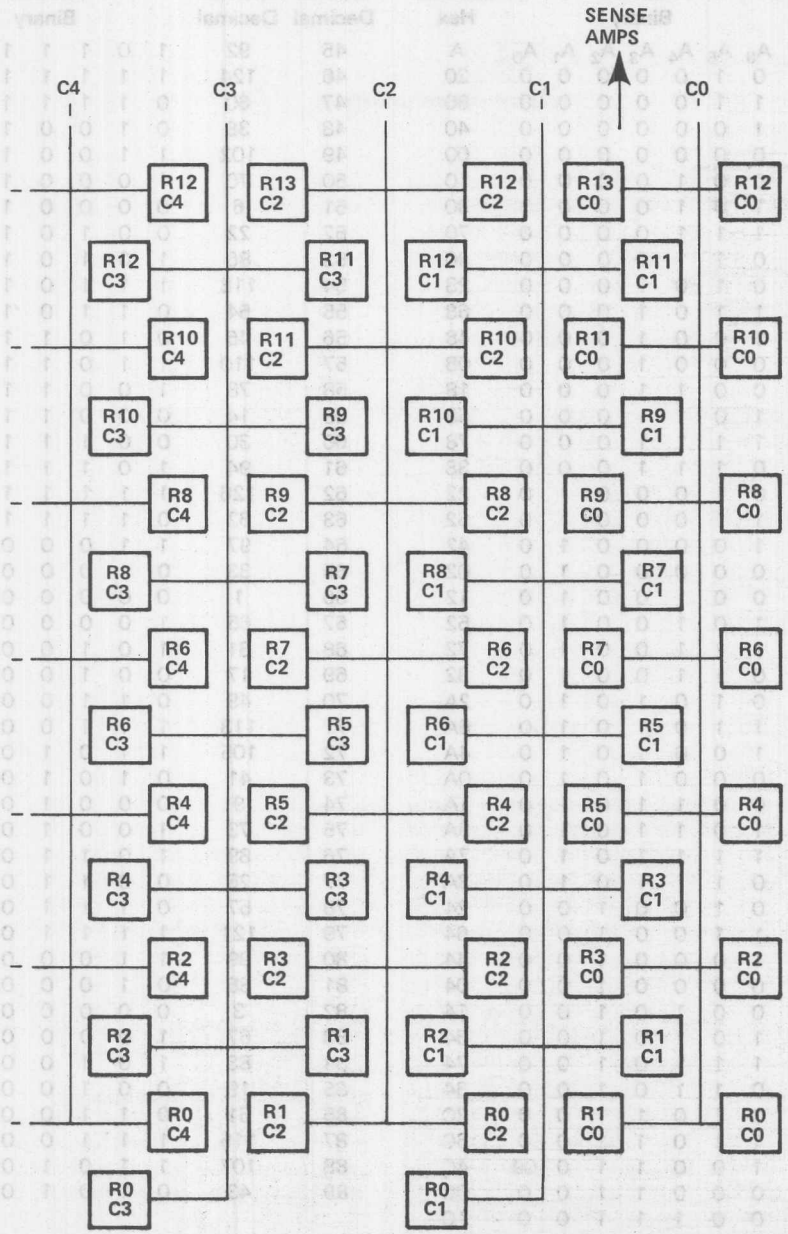
EXTERNAL TRANSFORMATION NECESSARY TO COUNTERACT THE INTERNAL INVERSION OF DATA WITHIN THE MK4116

Figure 3

(ROW ADDRESS MSB)

NOTE: The same transformation will be required on the D_{OUT} of the MK 4116. This data inversion is transparent to the user and need be considered only in testing of the MK 4116.

NOTE: The logic symbol  is used solely to indicate the logic function "Exclusive — OR". The above figure is not a suggested implementation of logic.



The area represented here is physically located in the lower right hand corner of the bottom half array. (See Figure 4)

MK4116 TOPOGRAPHICAL MAP ROW ADDRESS RELATIONSHIPS

Table 1

Internal Decimal	External Decimal	External Binary							External Hex
R	A	A_6	A_5	A_4	A_3	A_2	A_1	A_0	A
0	32	0	1	0	0	0	0	0	20
1	96	1	1	0	0	0	0	0	60
2	64	1	0	0	0	0	0	0	40
3	0	0	0	0	0	0	0	0	00
4	16	0	0	1	0	0	0	0	10
5	80	1	0	1	0	0	0	0	50
6	112	1	1	1	0	0	0	0	70
7	48	0	1	1	0	0	0	0	30
8	40	0	1	0	1	0	0	0	28
9	104	1	1	0	1	0	0	0	68
10	72	1	0	0	1	0	0	0	48
11	8	0	0	0	1	0	0	0	08
12	24	0	0	1	1	0	0	0	18
13	88	1	0	1	1	0	0	0	58
14	120	1	1	1	1	0	0	0	78
15	56	0	1	1	1	0	0	0	38
16	34	0	1	0	0	0	1	0	22
17	98	1	1	0	0	0	1	0	62
18	66	1	0	0	0	0	1	0	42
19	2	0	0	0	0	0	1	0	02
20	18	0	0	1	0	0	1	0	12
21	82	1	0	1	0	0	1	0	52
22	114	1	1	1	0	0	1	0	72
23	50	0	1	1	0	0	1	0	32
24	42	0	1	0	1	0	1	0	2A
25	106	1	1	0	1	0	1	0	6A
26	74	1	0	0	1	0	1	0	4A
27	10	0	0	0	1	0	1	0	0A
28	26	0	0	1	1	0	1	0	1A
29	90	1	0	1	1	0	1	0	5A
30	122	1	1	1	1	0	1	0	7A
31	58	0	1	1	1	0	1	0	3A
32	36	0	1	0	0	1	0	0	24
33	100	1	1	0	0	1	0	0	64
34	68	1	0	0	0	1	0	0	44
35	4	0	0	0	0	1	0	0	04
36	20	0	0	1	0	1	0	0	14
37	84	1	0	1	0	1	0	0	54
38	116	1	1	1	0	1	0	0	74
39	52	0	1	1	0	1	0	0	34
40	44	0	1	0	1	1	0	0	2C
41	108	1	1	0	1	1	0	0	6C
42	76	1	0	0	1	1	0	09	4C
43	12	0	0	0	1	1	0	0	0C
44	28	0	0	1	1	1	0	0	1C

Table 1 Continued

Internal Decimal	External Decimal	External Binary							External Hex
45	92	1	0	1	1	1	0	0	5C
46	124	1	1	1	1	1	0	0	7C
47	60	0	1	1	1	1	0	0	3C
48	38	0	1	0	0	1	1	0	26
49	102	1	1	0	0	1	1	0	66
50	70	1	0	0	0	1	1	0	46
51	6	0	0	0	0	1	1	0	06
52	22	0	0	1	0	1	1	0	16
53	86	1	0	1	0	1	1	0	56
54	118	1	1	1	0	1	1	0	76
55	54	0	1	1	0	1	1	0	36
56	46	0	1	0	1	1	1	0	2E
57	110	1	1	0	1	1	1	0	6E
58	78	1	0	0	1	1	1	0	4E
59	14	0	0	0	1	1	1	0	0E
60	30	0	0	1	1	1	1	0	1E
61	94	1	0	1	1	1	1	0	5E
62	126	1	1	1	1	1	1	0	7E
63	62	0	1	1	1	1	1	0	3E
64	97	1	1	0	0	0	0	1	61
65	33	0	1	0	0	0	0	1	21
66	1	0	0	0	0	0	0	1	01
67	65	1	0	0	0	0	0	1	41
68	81	1	0	1	0	0	0	1	51
69	17	0	0	1	0	0	0	1	11
70	49	0	1	1	0	0	0	1	31
71	113	1	1	1	0	0	0	1	71
72	105	1	1	0	1	0	0	1	69
73	41	0	1	0	1	0	0	1	29
74	9	0	0	0	1	0	0	1	09
75	73	1	0	0	1	0	0	1	49
76	89	1	0	1	1	0	0	1	59
77	25	0	0	1	1	0	0	1	19
78	57	0	1	1	1	0	0	1	39
79	121	1	1	1	1	0	0	1	79
80	99	1	1	0	0	0	1	1	63
81	35	0	1	0	0	0	1	1	23
82	3	0	0	0	0	0	1	1	03
83	67	1	0	0	0	0	1	1	43
84	83	1	0	1	0	0	1	1	53
85	19	0	0	1	0	0	1	1	13
86	51	0	1	1	0	0	1	1	33
87	115	1	1	1	0	0	1	1	73
88	107	1	1	0	1	0	1	1	6B
89	43	0	1	0	1	0	1	1	2B

Table 1 Continued

Internal Decimal	External Decimal	External Binary							External Hex
90	11	0	0	0	1	0	1	1	0B
91	75	1	0	0	1	0	1	1	4B
92	91	1	0	1	1	0	1	1	5B
93	27	0	0	1	1	0	1	1	1B
94	59	0	1	1	1	0	1	1	3B
95	123	1	1	1	1	0	1	1	7B
96	101	1	1	0	0	1	0	1	65
97	37	0	1	0	0	1	0	1	25
98	5	0	0	0	0	1	0	1	05
99	69	1	0	0	0	1	0	1	45
100	85	1	0	1	0	1	0	1	55
101	21	0	0	1	0	1	0	1	15
102	53	0	1	1	0	1	0	1	35
103	117	1	1	1	0	1	0	1	75
104	109	1	1	0	1	1	0	1	6D
105	45	0	1	0	1	1	0	1	2D
106	13	0	0	0	1	1	0	1	0D
107	77	1	0	0	1	1	0	1	4D
108	93	1	0	1	1	1	0	1	5D
109	29	0	0	1	1	1	0	1	1D
110	61	0	1	1	1	1	0	1	3D
111	125	1	1	1	1	1	0	1	7D
112	103	1	1	0	0	1	1	1	67
113	39	0	1	0	0	1	1	1	27
114	7	0	0	0	0	1	1	1	07
115	71	1	0	0	0	1	1	1	47
116	87	1	0	1	0	1	1	1	57
117	23	0	0	1	0	1	1	1	17
118	55	0	1	1	0	1	1	1	37
119	119	1	1	1	0	1	1	1	77
120	111	1	1	0	1	1	1	1	6F
121	47	0	1	0	1	1	1	1	2F
122	15	0	0	0	1	1	1	1	0F
123	79	1	0	0	1	1	1	1	4F
124	95	1	0	1	1	1	1	1	5F
125	31	0	0	1	1	1	1	1	1F
126	63	0	1	1	1	1	1	1	3F
127	127	1	1	1	1	1	1	1	7F

MK4116 TOPOGRAPHICAL MAP COLUMN ADDRESS RELATIONSHIPS

Table 2

Internal Decimal	External Decimal	External Binary							External Hex
0	64	1	0	0	0	0	0	0	40
1	0	0	0	0	0	0	0	0	00
2	32	0	1	0	0	0	0	0	20
3	96	1	1	0	0	0	0	0	60
4	80	1	0	1	0	0	0	0	50
5	16	0	0	1	0	0	0	0	10
6	48	0	1	1	0	0	0	0	30
7	112	1	1	1	0	0	0	0	70
8	72	1	0	0	1	0	0	0	48
9	8	0	0	0	1	0	0	0	08
10	40	0	1	0	1	0	0	0	28
11	104	1	1	0	1	0	0	0	68
12	88	1	0	1	1	0	0	0	58
13	24	0	0	1	1	0	0	0	18
14	56	0	1	1	1	0	0	0	38
15	120	1	1	1	1	0	0	0	78
16	66	1	0	0	0	0	1	0	42
17	2	0	0	0	0	0	1	0	02
18	34	0	1	0	0	0	1	0	22
19	98	1	1	0	0	0	1	0	62
20	82	1	0	1	0	0	1	0	52
21	18	0	0	1	0	0	1	0	12
22	50	0	1	1	0	0	1	0	32
23	114	1	1	1	0	0	1	0	72
24	74	1	0	0	1	0	1	0	4A
25	10	0	0	0	1	0	1	0	0A
26	42	0	1	0	1	0	1	0	2A
27	106	1	1	0	1	0	1	0	6A
28	90	1	0	1	1	0	1	0	5A
29	26	0	0	1	1	0	1	0	1A
30	58	0	1	1	1	0	1	0	3A
31	122	1	1	1	1	0	1	0	7A
32	68	1	0	0	0	1	0	0	44
33	4	0	0	0	0	1	0	0	04
34	36	0	1	0	0	1	0	0	24
35	100	1	1	0	0	1	0	0	64
36	84	1	0	1	0	1	0	0	54
37	20	0	0	1	0	1	0	0	14
38	52	0	1	1	0	1	0	0	34
39	116	1	1	1	0	1	0	0	74
40	76	1	0	0	1	1	0	0	4C
41	12	0	0	0	1	1	0	0	0C
42	44	0	1	0	1	1	0	0	2C
43	108	1	1	0	1	1	0	0	6C
44	92	1	0	1	1	1	0	0	5C

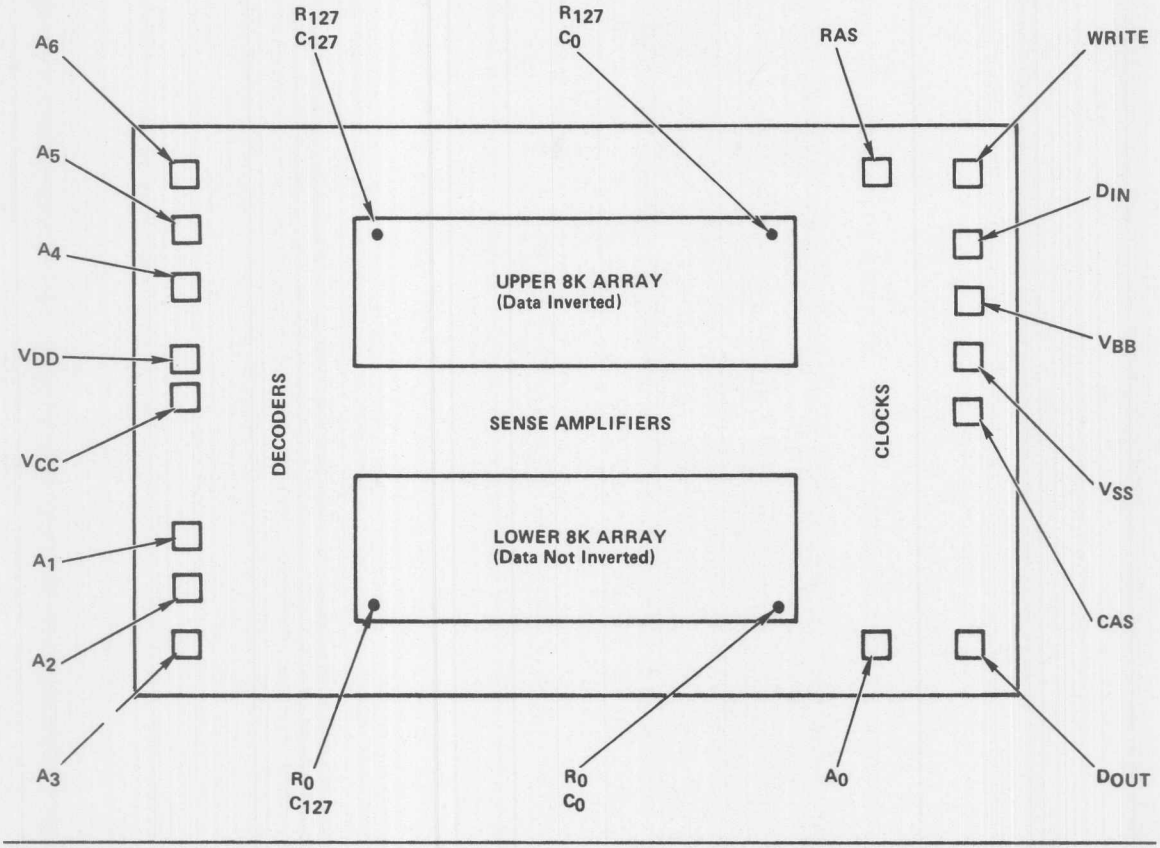
III

Table 2 Continued

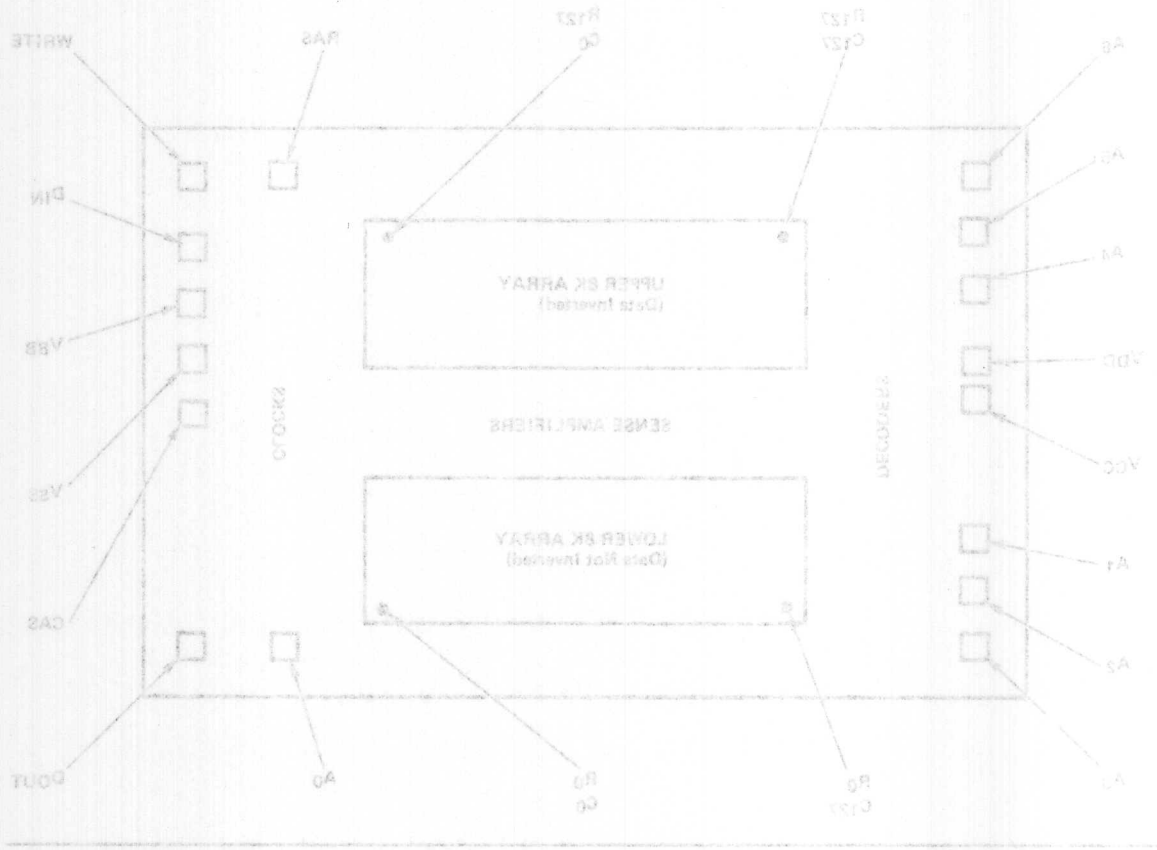
Internal Decimal	External Decimal	External Binary								External Hex
45	28	0	0	1	1	1	0	0		1C
46	60	0	1	1	1	1	0	0		3C
47	124	1	1	1	1	1	0	0		7C
48	70	1	0	0	0	1	1	0		46
49	6	0	0	0	0	1	1	0		06
50	38	0	1	0	0	1	1	0		26
51	102	1	1	0	0	1	1	0		66
52	86	1	0	1	0	1	1	0		56
53	22	0	0	1	0	1	1	0		16
54	54	0	1	1	0	1	1	0		36
55	118	1	1	1	0	1	1	0		76
56	78	1	0	0	1	1	1	0		4E
57	14	0	0	0	1	1	1	0		0E
58	46	0	1	0	1	1	1	0		2E
59	110	1	1	0	1	1	1	0		6E
60	94	1	0	1	1	1	1	0		5E
61	30	0	0	1	1	1	1	0		1E
62	62	0	1	1	1	1	1	0		3E
63	126	1	1	1	1	1	1	0		7E
64	65	1	0	0	0	0	0	1		41
65	1	0	0	0	0	0	0	1		01
66	33	0	1	0	0	0	0	1		21
67	97	1	1	0	0	0	0	1		61
68	81	1	0	1	0	0	0	1		51
69	17	0	0	1	0	0	0	1		11
70	49	0	1	1	0	0	0	1		31
71	113	1	1	1	0	0	0	1		71
72	73	1	0	0	1	0	0	1		49
73	9	0	0	0	1	0	0	1		09
74	41	0	1	0	1	0	0	1		29
75	105	1	1	0	1	0	0	1		69
76	89	1	0	1	1	0	0	1		59
77	25	0	0	1	1	0	0	1		19
78	57	0	1	1	1	0	0	1		39
79	121	1	1	1	1	0	0	1		79
80	67	1	0	0	0	0	1	1		43
81	3	0	0	0	0	0	1	1		03
82	35	0	1	0	0	0	1	1		23
83	99	1	1	0	0	0	1	1		63
84	83	1	0	1	0	0	1	1		53
85	19	0	0	1	0	0	1	1		13
86	51	0	1	1	0	0	1	1		33
87	115	1	1	1	0	0	1	1		73
88	75	1	0	0	1	0	1	1		4B
89	11	0	0	0	1	0	1	1		0B

Table 2 Continued

Internal Decimal	External Decimal	External Binary								External Hex
90	43	0	1	0	1	0	1	1		2B
91	107	1	1	0	1	0	1	1		6B
92	91	1	0	1	1	0	1	1		5B
93	27	0	0	1	1	0	1	1		1B
94	59	0	1	1	1	0	1	1		3B
95	123	1	1	1	1	0	1	1		7B
96	69	1	0	0	0	1	0	1		45
97	5	0	0	0	0	1	0	1		05
98	37	0	1	0	0	1	0	1		25
99	101	1	1	0	0	1	0	1		65
100	85	1	0	1	0	1	0	1		55
101	21	0	0	1	0	1	0	1		15
102	53	0	1	1	0	1	0	1		35
103	117	1	1	1	0	1	0	1		75
104	77	1	0	0	1	1	0	1		4D
105	13	0	0	0	1	1	0	1		0D
106	45	0	1	0	1	1	0	1		2D
107	109	1	1	0	1	1	0	1		6D
108	93	1	0	1	1	1	0	1		5D
109	29	0	0	1	1	1	0	1		1D
110	61	0	1	1	1	1	0	1		3D
111	125	1	1	1	1	1	0	1		7D
112	71	1	0	0	0	1	1	1		47
113	7	0	0	0	0	1	1	1		07
114	39	0	1	0	0	1	1	1		27
115	103	1	1	0	0	1	1	1		67
116	87	1	0	1	0	1	1	1		57
117	23	0	0	1	0	1	1	1		17
118	55	0	1	1	0	1	1	1		37
119	119	1	1	1	0	1	1	1		77
120	79	1	0	0	1	1	1	1		4F
121	15	0	0	0	1	1	1	1		0F
122	47	0	1	0	1	1	1	1		2F
123	111	1	1	0	1	1	1	1		6F
124	95	1	0	1	1	1	1	1		5F
125	31	0	0	1	1	1	1	1		1F
126	63	0	1	1	1	1	1	1		3F
127	127	1	1	1	1	1	1	1		7F


A6
A5
A4
VDD
VCC
A1
A2
A3
R127
C127
R0
C127
R127
C0
R0
C0
RAS
A0
WRITE
DIN
VBB
VSS
CAS
DOUT
UPPER 8K ARRAY
(Data Inverted)
SENSE AMPLIFIERS
LOWER 8K ARRAY
(Data Not Inverted)
DECODERS
CLOCKS

III


WRITE
RAS
DIN
VBB
VSS
CAS
DOUT
A0
A9
A8
A7
A6
A5
A4
VDD
VCC
A3
A2
A1
UPPER BK ARRAY
(Data Inverted)
SENSE AMPLIFIERS
LOWER BK ARRAY
(Data Not Inverted)

MK4116 POST BURN-IN FUNCTIONAL TEST DESCRIPTION

Testing

This defines the functional test sequence used by MOSTEK for post burn-in final testing of its 16384 bit dynamic randon-access memory, the MK 4116. The same sequence, with Test No. 4 deleted, is used for the QC audit performed immediately prior to shipment, and for periodic readings during all life test studies performed by MOSTEK. The testers used for all such testing at MOSTEK are Siemens 203 (or an earlier version of the same basic tester, the Computest V200).

The test temperature is an equivalent junction temperature for operation at 70°C continuous still air ambient as calcualted from the equation

$$T_J = T_A + P_D \theta_{JX}.$$

Any parameter which is not worst-case at the elevated temperature is compensated to account for variation over the 0°C–70°C specified operating temperature range.

All timing edges are set to data sheet limits plus or minus guardband deltas where appropriate; the power supplies are set to the minimum and maximum data sheet limits plus or minus appropriate guardband deltas (with the exception of V_{CC} which set to the minimum data sheet level only). Input levels are

V_{IH} = minimum data sheet limit minus guard-band delta.

V_{IHC} = minimum data sheet limit minus guard-band delta.

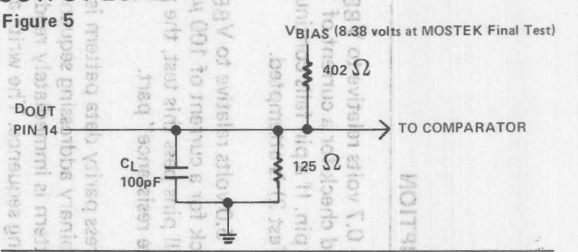
V_{IL} = maximum data sheet limit plus guard-band delta.

unless otherwise noted. The output load is as shown in the attached figure.

MOSTEK reserves the right to make changes in this test sequence at any time and without notice.

OUTPUT LOAD

Figure 5



III

TEST NO.	TITLE	DESCRIPTION	REASON
1	Continuity (low bias)	Force – 0.7 volts relative to V_{BB} on each pin in turn, and check for a current of 100 μA or greater on each pin. If a pin fails continuity, High Bias Continuity (Test 2) is attempted.	
2	Continuity (high bias-attempted only if Test 1 fails)	Force – 5.0 volts relative to V_{BB} on each pin in turn, and check for a current of 100 μ A or greater on each pin. If all pins pass this test, the part is rejected as a "high substrate resistance" part.	
3	Pre-stress	An address parity data pattern is written into the matrix using a binary addressing sequence (rows fast). The data pattern is immediately read back using the same addressing sequence. The write and read sequences are repeated for data complement.	This test checks for minimum functionality.
4	Stress	Multiple runs are made using a procedure the same as Test 3 except that errors are ignored and the voltage between the power supplies is increased.	Places maximum field intensity across gate oxides.
5	Post-stress	Same as Test 3	This test checks to see if the stress either destroyed or latched up the part.
6	I_{DD} operating (average) (I_{DD1})	With V_{BB} at the data sheed minimum and V_{DD} at the data sheet maximum, measure I_{DD} (average) while repetitively writing "zero" at location (0,0) at minimum t_{RC}. Reject the part of the measured value exceeds I_{DD2} (max).	
7	Substrate Leakage (I_{BB2})	All pins other than V_{BB} are grounded. V_{BB} is biased at –20 volts through the meter and checked for less than 10 μA leakage current.	

TEST NO.	TITLE	DESCRIPTION	REASON
8	Input Leakage ($I_{I(L)}$)	V_{BB} is biased at −5 volts with respect to all other supplies, ground, and the output pin. All inputs are forced to 0 volts and the current measured on each individual input is considered a failure if it exceeds 7 μA magnitude. 10 volts is then forced sequentially on each input, and the current is again measured to the same fail condition.	
9	I_{DD} Standby	The device is powered up with minimum V_{BB}, maximum V_{DD}, and maximum V_{CC}. The output is left floating and unused inputs are forced to 0 volts. Multiple toggles between 5 volts and 0 volts are applied to $\overline{RAS}$ and $\overline{CAS}$; after toggling $\overline{RAS}$ and $\overline{CAS}$ are at 5 volts. The maximum I_{DD} in the standby state is then measured.	
10	Output Leakage ($I_{O(L)}$)	The device is powered up with maximum V_{DD}, maximum V_{CC}, and minimum V_{BB}. Unused inputs are forced to 0 volts. Multiple toggles between 5 volts and 0 volts are applied to $\overline{RAS}$ and $\overline{CAS}$; after toggling, $\overline{RAS}$ and $\overline{CAS}$ are at 5 volts. 5.5 volts is connected to the output pin through the meter, and the current is measured against a failure condition of leakage greater than 7 μA. The output pin is then forced to 0 volts and the current is again measured against the same failure conditions.	
11	VBUMP	At minimum V_{DD} and maximum V_{BB} the entire matrix is written to discharge cells. The V_{DD} and V_{BB} supplies are then slewed in the positive direction, and the entire matrix is read for discharge cells.	This test verifies pr sense amp margins for detection of low stc states.
12	Start-up — Address Parity	After powering up all supplies from 0 volts, eight $\overline{RAS}$-only cycles at maximum cycle time are executed before the entire matrix is written with complement data using a binary addressing sequence (rows fast). It is then read for complement data, written with true data, and finally read for true data using the same addressing sequence.	This test checks that internal circuitry is adequately initialized 8 preliminary cycles.

TEST NO.	TITLE	DESCRIPTION	REASON
13	TMOD-Diagonal	The entire matrix is written to a background of complement data. Using a binary addressing sequence (rows fast) the matrix is written using cycles with $\overline{RAS}$ and $\overline{CAS}$ active pulse widths of 10μSEC. There is a standby stall executed after each column has been written to finish the refresh limit interval. The matrix is then read using the same length cycles and addressing scheme with no standby stalls. The procedure is repeated for complement data.	This test checks both the ability to write and the validity of the output data at the end of a long active cycle. It checks the ability of the row decoders to hold the 127 non-selected row lines "OFF" during a long active cycle, and the ability of the sense amplifiers to read a single bit in a field of complement data.
14	YFAST-Rows 0, 63, 64, 127	Using a binary addressing sequence in a column fast mode, the matrix is written with data until the refresh limit interval is reached. At that time each row is refreshed using a single $\overline{RAS}$-only cycle. The entire matrix is written, read, written with complement data, and read for complement data is this matter.	This test checks for column decoder noise effects on the sense amps and for the other noise related failure modes.
15	Page Mode-Address Parity	Using a binary addressing sequence (rows fast), the entire matrix is written to a background of zeroes. For the number of page cycles that can be executed during the $\overline{RAS}$ active time of 10μ seconds, each row is written with true data. A portion of all 128 rows is written, read, written with complement data, and read for complement data using page mode. This procedure is repeated for a new set of addresses until the entire matrix has been finished. Finally using a normal cycle binary addressing sequence (rows fast) the entire matrix is read for complement data.	This test checks reading, writing, and duration of page mode operation. It also checks the refresh limit interval.
16	Early $\overline{CAS}$, Late $\overline{Write}$-Displaced double checkerboard	Using a binary addressing sequence (rows fast) throughout this test, the entire matrix is written with complement data, written with true data,	This test checks for the refresh limit during an inactive stall as well as "Early

TEST NO.	TITLE	DESCRIPTION	REASON
		read for true data, and written with complement data using normal cycles. Using a late write cycle, the matrix is read for complement data and written with true data in the same cycle. After the entire matrix is written, a standby stall is executed for the refresh limit interval. Using a late write cycle, the matrix is read for true data and written with complement data in the same cycle. Another standby stall for the refresh limit interval follows. The matrix is read for complement data using normal cycles. Finally, the entire matrix is written with true data, read, written with complement data, and read for complement data using cycles with minimum t_{RCD}.	$\overline{CAS}$" and "Late $\overline{Write}$" modes of operation.
17	Address Complement-Horizontal Bars	Using a rows fast, complement addressing sequence (address, address complement, address + 1, . . .), the entire matrix is written, read, written with complement data, and read for complement data.	This test checks the integgrity of the address latches and decoders using an addressing sequence which generates many transitions on all address inputs.
18	March-Ones	Using a binary addressing sequence (rows fast), the entire matrix is written with true data. The matrix is then scanned by first reading a cell, then writing it with complement data, and finally reading it for complement data before proceding to the next cell location. The memory is scanned again by reading a cell for complement data, then writing it with true data, and finally reading it for true data before proceding to the next cell location. The procedure is then repeated with the addresses complemented during an identical data and data complement sequence.	Checks for address uniqueness.
19	March-Checkerboard	Same as Test 17.	

TEST NO.	TITLE	DESCRIPTION	REASON
20	High Impedance Output State	Using a binary addressing sequence (rows fast), the entire matrix is written with ones and the output is checked to be in an open-circuit state. Next, while the entire matrix is read, the output is checked to be in an open-circuit state during the time $\overline{CAS}$ is in precharge. The procedure is repeated with zeroes as the data.	This test checks the c circuit state of D_{OU}
21	Vertical Bar	Using a binary addressing sequence (rows fast), the entire matrix is written to a background of complement data. Then the matrix is written with complement data, and finally read for complement data.	Checks for column de or adjacent bit interac
22	Vertical Bar; Wide inputs	This test is the same as Test 20 except input signal levels are at the data sheet extremes.	
23	Double Checkerboard	Same as Test 20	
24	Ones	Same as Test 20	
25	Walking Diagonal	This is the same as Test 20 except the test is run with the diagonal in all 128 possible positions.	
26	Matrix High	Using a binary addressing sequence (rows fast), all the cells in the matrix are written to a charged state. For the refresh limit interval an attempt is made to disturb half the matrix by generating write cycles which use column fast complement addressing. The test half of the matrix is then read for charged cells. The other half of the matrix is tested for the refresh with the same procedure (the disturbs generated use column fast addressing).	This test checks refi in a dynamic disturb environment.

TEST NO.	TITLE	DESCRIPTION	REASON
27	Matrix Low	This is the same as Test 25 except the cells in the matrix are written to the discharged state and the disturb time is 100 milliseconds.	This test checks for faulty gate oxides which allow discharged cells to leak toward V_{DD}.
28	t_{CRP}-Address Parity	This is the same as Test 20 except that $\overline{CAS}$ goes into precharge (logic 1) after $\overline{RAS}$ goes active (logic 0), and the output is checked for a continued valid condition for the duration of the $\overline{CAS}$ active time.	This test checks that the output remaining is dependent only on $\overline{CAS}$ remaining active (logic 0) and is independent of $\overline{RAS}$ returning to the inactive (precharge: logic 1) state.

TEST NUMBER	PARAMETERS CHECKED
All functional Tests (additional parameters are listed below)	t_{RAC}, t_{CAC}, t_{RP}, t_{RAS} (min), t_{RSH} t_{CSH}, t_{CAS} (min), t_{RCD} (max), t_{RSH} t_{RAH}, t_{ASC}, t_{CAH}, t_{WP}, t_{DS}, t_{DH}
Test 11	t_{RWL}, t_{CWL}
Test 12	t_{RAS} (max), t_{CAS} (max), t_{RWL}, t_{CWL}, t_{REF}
Test 13	t_{RWL}, t_{CWL}, t_{REF}
Test 14	t_{RCS}, t_{RCH}, t_{WCH}, t_{CP}, t_{REF}, t_{RAS} (max)
Test 15	t_{RCD} (min), t_{RCS}, t_{RCH}, t_{WCH}, t_{WCR}, t_{DHR}, t_{REF}, t_{CWD}, t_{RWD}
Test 16, 17, 18 20, 21, 22 23, 24, 26	t_{RCS}, t_{RCH}, t_{WCH}, t_{WCR}, t_{DHR}
Test 19	t_{OFF} (max), t_{WCS}
Test 20	t_{RCS}, t_{RCH}, t_{WCH}, t_{WCR}, t_{DHR}, t_{REF}
Test 27	t_{CRP}

OPTIMIZED TESTING OF 16K RAMS

Testing

The new generation of 16K dynamic MOS memories places a much greater burden on the test engineer than did the earlier 1K and 4K designs. The size of the memory means that generalized test sequences which test these devices as black boxes will be far too expensive in terms of test time per device. Even though the semiconductor industry appears to have standardized on one compatible pin-out with the major controversies being decided in favor of 128 – cycle refresh and output latch controlled by the column address strobe as in the MOSTEK MK 4116, there are pitfalls for the user who does not appreciate the fact that vendor design and testing differences will result in devices with different characteristics. Test sequences which do not comprehend these differences will not be successful in eliminating marginal devices. Therefore, the test engineer must acquire an in-depth knowledge of each vendor's device and the test sequences utilized must reflect this knowledge.

The following table illustrates graphically the test time penalties paid in moving from 4K to 16K:

	Test times for various test patterns (375 ns cycle)	
	N=4096	N=16384
2N (Load-Read)	3 mS	12 mS
$2N^{3/2}$ (Moving pattern, row or column ping-pong)	197 mS	1. 6 Sec
$2N^2$ (Ping-pong) GALPAT)	12. 6 Sec	201 Sec

When testing the 4K RAM, the test engineer could treat the device as a black box, generate all address transitions by using N^2 patterns, and hope for the best. Using such an approach on the 16K would result in a tester throughput of fewer than 400 parts per day.

TEST TEMPERATURE

The single most important decision to be made concerning dynamic RAM testing is test temperature. MOS devices have three basic parameters which are functions of temperature: threshold voltage, carrier mobility, and leakage currents. For N-channel silicon gate processes, threshold voltage is typically 200 millivolts lower at 100°C than at 0°C. Carrier mobility, which relates to transistor gain and therefore to circuit speed, is about 25% lower at 100°C than at 0°C. The effects of these two variables, once characterized for a particular device, may be easily included by adjusting parameters such as input and output levels for the temperature range variations expected. A third variable, leakage current, is more dramatic in its effect on the device.

The refresh time of any dynamic MOS Memory may be expressed by

$$t_{REF}=Ae^{-BT}$$

where T is junction temperature in °C
B is a variable relating the magnitude of the generation – recombination current to the junction temperature (units of 1/°C)

and A is a scaling constant reflecting such variables as junction area, sense amplifier design, bulk defect density.

Typical values for the variable B range from 0.053/ °C to 0.060/° C implying a temperature behavior in which refresh time is halved for every 11.6 °C to 13.1° C increase in junction temperature.

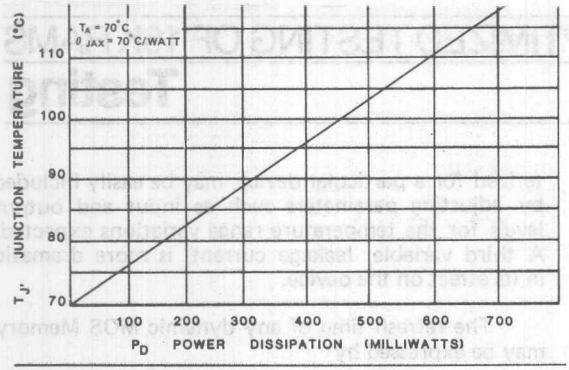
Testing should be conducted at elevated temperatures in order that this large variation may be tested without having to extrapolate from some non-worst-case temperature. (Since mobility is also worst-case at elevated temperature, most timing parameters are also worst-case at elevated temperatures and need not be guardbanded.)

Most 16K RAMS are specified over the temperature range 0 ° C to 70 ° C ambient. The junction temperature T_J depends, however, on the power dissipation (P_D) of the device by the equation

$$T_J=T_A+P_D\theta_{JAX}$$

Where θ_{JAX} is the thermal impedance between the device junction and system ambient. Figure 1 graphs this equation for θ_{JAX}=70 °C per watt (standard 16 pin ceramic dual in line package).

If the device junction temperature is stabilized by using a long warm-up cycle prior to the first test, the proper test temperature is the system ambient temperature. If the test is short enough that the junction temperature does not rise appreciably under test, the proper test temperature is the junction temperature given in Figure 1. For example, a device which dissipates 430 mW must be tested at T_J=100°C in order to guarantee functionality at T_A=70 °C.



THE MOSTEK MK 4116

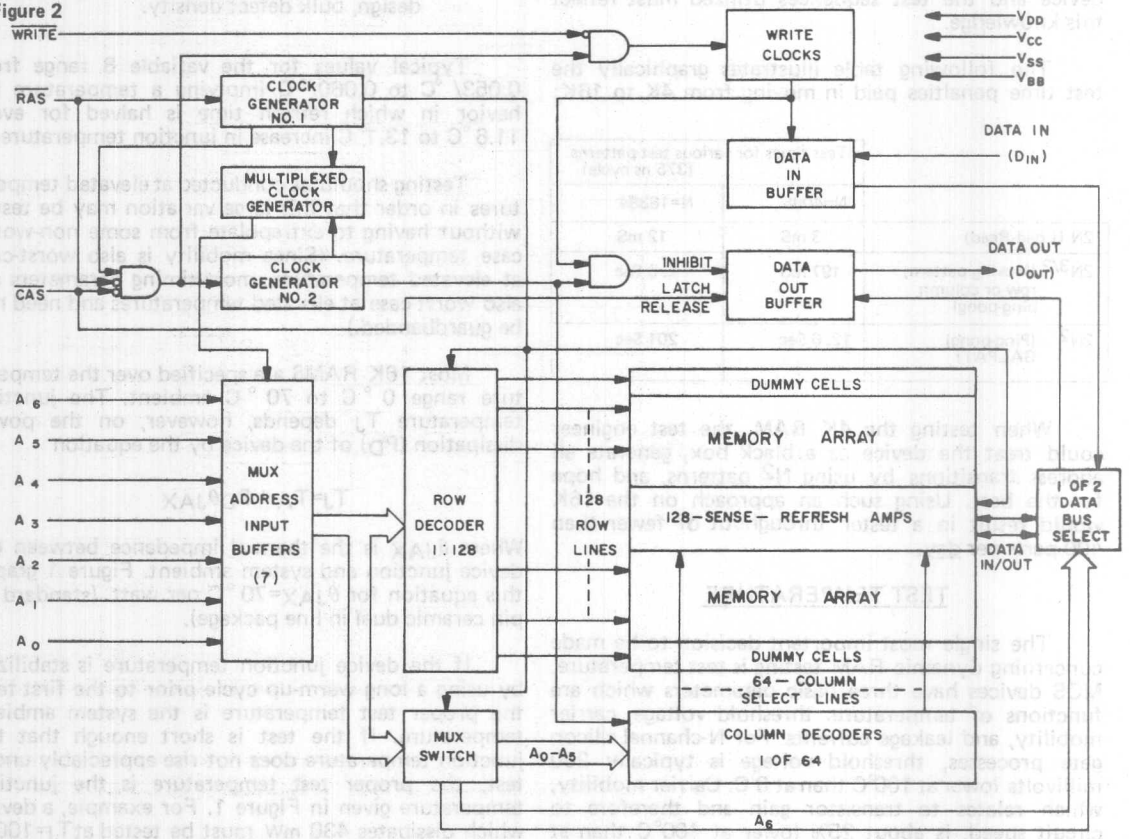
The block diagram of the MOSTEK MK 4116 (Figure 2) may be examined for testing implications. Note that the address input buffers are shared while the row and column decoders are independent. An addressing scheme which provides the maximum possible number of bit reversals per cycle will check

Note further that the data out buffer is timed exclusively by an internal clock generator driven by $\overline{CAS}$. There is no reason, then, to search for some test sequence or data pattern which is "worst-case" for the access time. Access time is absolutely determined by clock delays internal to the circuit and is only influenced by influencing these delays. Access time, along with most other timing parameters is worst-case at low V_{DD} (+10.8 volts). V_{BB} has almost no influence on access time.

Still referring to Figure 2, note that there are two 8K sub-arrays split by the sense-refresh amplifiers in the middle and having "dummy cells" at each side. These establish a voltage reference for the balanced sense amplifiers. One of the array halves, therefore, inverts data and will store an input "one" as a low level in the storage cell (a second inversion is performed by the output circuitry so that this internal inversion is not seen at the device terminals). This inversion must be taken into account when performing a refresh test.

BLOCK DIAGRAM MK4116

Figure 2



The layout of the storage cell in the MK 4116 is shown in Figure 3. This is a conventional one-transistor dynamic storage cell, although implemented by using MOSTEK's double-level polysilicon (Poly II™) process. The row (word) select lines are metal, eliminating concern over propagation delays down the long 80 mil word lines. Data transfer to and from the cell is through the diffused column (digit) lines. The top plate of the storage capacitor is V_{DD} (first level of polysilicon) which allows charge to be stored in the depleted region beneath this level. Metal word lines contact the second poly level which forms the gate of the transfer device isolating the storage cell from the digit line. The cell is relatively insensitive to variations in the doping level of both first and second poly. In fact, performance of the cell is primarily influenced by junction depth, oxide thickness, and mask geometry, all parameters which tend to remain constant.

MK4116 CELL LAYOUT

Figure 3

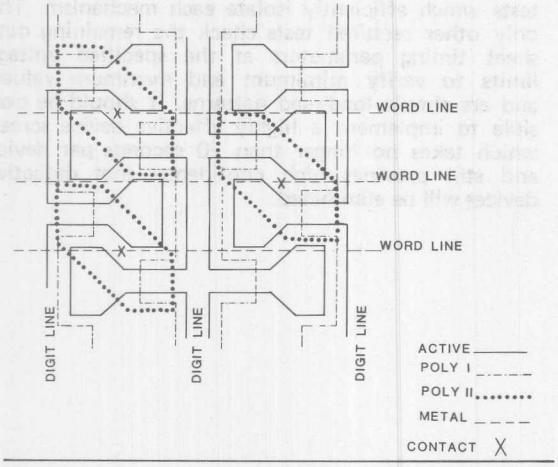
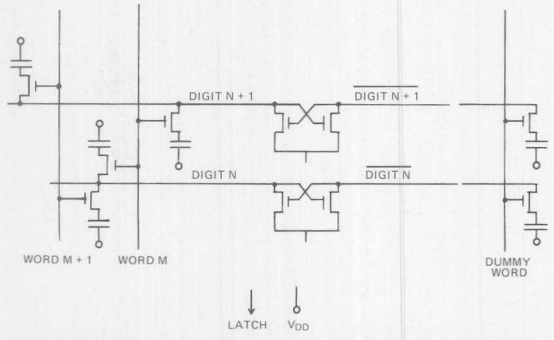


Figure 4 relates the cell, sense amplifier, and dummy cells. This figure provides a measure of topological information in addition to the electrical schematic. Capacitor-to-capacitor adjacencies in Figure 4 were carefully drawn to reflect the physical relationship of the actual layout.

MK4116 CELL, DUMMY CELL, SENSE AMPLIFIER

Figure 4



Because of the cell layout, tests to eliminate bit-to-bit sensitivities need to be considered carefully. The conventional "checkboard" pattern will result in an alternating bit-by-bit data pattern, as usual, but a "vertical bar" pattern consisting of alternate columns of highs and lows will accomplish the same result.

Two neighboring bits which might influence one another may be located on the same row or be separated by one row, but will not be on adjacent rows. Such bits must be on adjacent columns. There is also a topological mapping in the decoder layout which must be considered if rows and columns are to be accessed in a sequential manner.

SENSE AMPLIFIER MARGIN

Sense amp operation is straightforward:

1. Digit and $\overline{\text{Digit}}$ lines are precharged high, word lines and the dummy cell are precharged low, and LATCH is precharged high.
2. The selected word line turns on to V_{DD} along with the dummy word line accessing the dummy cells in the array half which does not contain the accessed cells. The accessed cells are thus connected via the transfer gates to the digit and $\overline{\text{digit}}$ lines. Charge redistribution between the cells and digit lines causes a voltage drop on the digit line of zero to 0.3 volts if the cell contained a high level (depending on the amount of decay in the cell since the last access), or of about 0.5 volts if the cell was initially low. The dummy cell pulls the $\overline{\text{digit}}$ line down by 0.4 volts.
3. Latch is driven to ground allowing the balanced sense amplifier to discharge the digit or $\overline{\text{digit}}$ line, whichever started at the lower voltage.

Accessing a stored low level requires that the digit line be discharged by the cell, whereas accessing a stored high level is accomplished whenever the digit line is relatively undisturbed.

Design and layout of the storage array and sense amplifier is complicated by the presence on critical nodes of noise which adds to or subtracts from signal voltages, causing a data-dependent reduction in overall margin. The data pattern which creates worst-case coupling and smallest margins in the MK 4116 is a solid field of discharged cells.

Insufficient precharge of the sense amplifier, which can arise from several distinct types of processing defects, causes the result of the current cycle to depend upon the preceding cycle. One data pattern which efficiently checks for such failure modes is the "major diagonal" or its extension, the $2N^{3/2}$ "moving diagonal". Beginning with a major diagonal of ones in a field of zeroes, each successive pass through the memory moves the diagonal up one

position such that in 128 passes it has occupied every possible position. Each bit has then been the only high in a row and column of low bits.

REFRESH TESTING

Refresh tests may be roughly divided into two subgroups – active and static. Active refresh indicates that the device is continuously operated for the period during which the unaddressed row or rows is allowed to decay.

Such a test provides an opportunity for increased cell leakage, either by sub-threshold conduction through transfer gates whose word line has been driven slightly positive due to noise coupling, by cell to cell leakage if the disturbing cycles are conducted on adjacent cells, or by charge carriers injected into the substrate by some nearby node. On the other hand, a static refresh test in which both $\overline{RAS}$ and $\overline{CAS}$ remain inactive for the entire refresh interval allows internally precharged nodes to decay. Such a test insures that, in addition to data being retained for the refresh interval, the peripheral circuits are also functioning after the pause.

If the refresh tests are being conducted at elevated temperatures with a stable junction temperature, the worst voltage corner for refresh is low V_{DD} (10.8 volts) and high V_{BB} (–5.5 volts). If the devices are allowed to self-heat prior to testing, then the high V_{DD} (13.2 volt) corner provides maximum power dissipation, maximum junction temperature, and minimum refresh time. In any event, high V_{BB} results in higher leakage current and shorter refresh times.

DECODER AND I/O

In addition to functional tests to check for the failure modes just described it is, of course, necessary to verify proper operation of the decoders and the input and output of data. Here no special techniques are required beyond those widely utilized in industry 1K and 4K RAM testing since this functionality may be proven with simple 2N tests. In fact, testing of the MK 4116 with its data output latch controlled exclusively by $\overline{CAS}$ is much simpler since there is no influence on the current cycle by a previous cycle as is the case for latched output designs. Parametric tests verifying input and output leakage specifications are also identical to that required by 4K devices, although here again the control of data out by $\overline{CAS}$ simplifies the output leakage measurement.

SUMMARY

Some of the basic failure mechanisms of the MK 4116 have been explained, along with suggested tests which efficiently isolate each mechanism. The only other required tests check the remaining data sheet timing parameters at the specified voltage limits to verify mimimum and maximum values, and are simple load-read patterns. It should be possible to implement a highly effective device screen which takes no longer than 20 seconds per device and still provides high confidence that defective devices will be eliminated.

A TESTING PHILOSOPHY FOR 16K DYNAMIC MEMORIES

Testing

Today several semiconductor manufacturers are moving 16384 bit dynamic MOS memories into volume production. The circuit will be the most cost-effective method of providing medium performance, large capacity randomly accessible data storage over the next several years and will in all likelihood be shipped in larger volume to more users than has any previous memory chip. This burgeoning market will confront many engineers with the problems of performing comparative evaluations, writing incoming device tests, system and diagnostic tests, and field troubleshooting and repair of memory systems containing many 16K chips. A thorough understanding of the device permits the engineer to evaluate the adequacy of manufacturers' outgoing screens and, if necessary,, to institute efficient incoming tests which comprehend the differences or shortcomings in the individual designs or outgoing test procedures.

Since the 16K has established the state-of-the-art in MOS design and processing at this point in time, the test sequences utilized must be carefully considered to keep test times to a reasonable minimum while at the same time adequately screening out marginal devices. The testing considerations themselves are applicable to earlier 1K and 4K circuits as well; the penalties for inadequacy are greater.

A brief description of manufacturing test procedures which relate ultimately to the quality and reliability of the memory chip would include characterization tests, in which the processing constraints and operating limits of a specific design are determined; reliability tests, which subject production lots to abnormal stresses in order to convert latent defects into failures prior to the final test; and the final test itself in which the manufacturer must always tread a thin line between test throughput (minimum test cost per device) and thoroughness. The quality of these tests varies from manufacturer to manufacturer and is manifested in the quality of their shipped product. Good design and quality processing are not enough, alone, to guarantee reliability; they must always be augmented by adequate testing.

BASIC CONSIDERATIONS

The storage element in all 16K RAMs is an MOS capacitor with data transfer and isolation controlled by a single transistor. This is the well known single transistor (1T) cell, used for the first time in the 4K memory devices which have been available for several years. The small size of the cell (about 0.7 mil^2 when fabricated in the double level polysilicon process) is sufficient inducement that the disadvantages are tolerated by the designer. Read-out is destructive, requiring an internal restore operation after each read. Available signal levels are dictated by the ratio of cell to digit line capacitance and are on the order of one to two hundred millivolts. Charge storage is of course dynamic in nature, since the charge stored on the capacitor will eventually leak off.

Storage time is an intrinsic device parameter; refresh time (more properly refresh interval) is a timing parameter which specifies the maximum allowable interval separating two operations on the same storage location which will re-establish the full charge on a partially-decayed high level.

The storage time of any dynamic MOS RAM may be expressed by the empirical equation

$$t_{STORAGE} = A \exp(-BT)$$

where

T is junction temperature in °C

B is a variable relating the magnitude of the generation-recombination current to the junction temperature (units of 1/°C)

and

A is a scaling constant reflecting such variables as junction area, bulk defect density, and sense amplifier design.

Note that the term "B" in the equation is not a constant. Conventionally it is assumed that the storage time doubles for every 10 °C decrease in junction temperature, which is equivalent to assuming that B = 0.069. Data shows that a typical value for B is 0.055, but that it does in fact vary at least 30% from this typical value. This equation is graphed in Figure 1 for several different values of B, arbitrarily assuming a minimum storage time of 2 milliseconds at T_J = 100°C. The storage time at T_J = 25°C for this hypothetical device will lie somewhere between 50 milliseconds and 381 milliseconds. If room temperature testing is to be attempted, the refresh interval would have to be set at 381 milliseconds, since any lesser value would not guarantee 2 milliseconds at 100° C. The devices which failed such a test would

the number of good devices found by the first screen, but in general the number of units requiring a second test is so great that the first screen may as well be eliminated in favor of a 100% screen at the maximum junction temperature.

Storage time is of course not the only parameter of interest. Other parameters which need to be verified over the temperature range include access time, power dissipation, and input/output levels. Access time and power dissipation are functions of transistor gain. Gain is temperature dependent through carrier mobility and is about 25% lower at 100 °C than at 0 °C. Access time is therefore worst-case at elevated temperatures. The memory will dissipate more power at low temperature, although much of the power required is capacitive and therefore frequency rather than temperature related. Signal levels are functions of transistor threshold voltage, which decreases about two millivolts for every 1 °C increase in temperature. Input high levels and output high and low levels are normally worst-case at low temperature and must be guardbanded if tested only at high temperature. (One 16K RAM, the MOSTEK MK 4116, utilizes an integrated reference voltage for address and data inputs which removes the threshold voltage dependence and therefore the temperature dependence of these inputs.) As will be discussed later, a few timing parameters become worst-case as the memory becomes faster, and need to be guardbanded if testing only at high temperature. On balance, however, due primarily to the extreme variation of storage time with temperature, it is most practical to conduct tests at the maximum junction temperature only and guardband non-worst-case parameters.

The two junction temperatures singled out in Figure 1 were not chosen at random. The equation describing temperature rise over an ambient is

$$T_J - T_A = \Delta T = \theta_{JA} P_D$$

where

θ_{JA} is the junction to ambient thermal resistance (for 16 pin ceramic DIP mounted in a socket on a double-sided PC board, the most widely accepted value is 70 °C/watt)

and

P_D is the power dissipation of the device under the conditons of interest.

I_{DD} (ACTIVE) = 30 MA
I_{DD} (STANDBY) = 1.5 MA
V_{DD} (MAXIMUM) = 13.2V
t_{cycle} = 375 ns

and assume that the refresh test is conducted by writing 16384 bits at the 375 ns cycle rate, pausing in the standby condition for the refresh interval, then reading all bits again at 375 ns. The rise in junction temperature can now be calculated:

$$t_{REFRESH} = 2\text{ms; duty factor (DF)} = \frac{2(16384)375\text{ns}}{2(16384)375\text{ns} + 2\text{ms}} = 0.86$$

$$\Delta T = \theta_{JA} (P_D \text{ ACTIVE (DF)} + P_D \text{ STANDBY } (1 - \text{DF}))$$

$$= 70\ ^\circ\text{C/W } (0.035\ (13.2)\ 0.86 + 0.0015\ (1 - 0.86))$$

$$= 28^\circ\text{C}$$

$$t_{REFRESH} = 381\text{ms; duty factor (DF)} = \frac{2(16384)375\text{ns}}{2(16384)375\text{ns} + 381\text{ms}} = 0.03$$

$$\Delta T = 70^\circ\text{C/W } (0.035\ (13.2)\ 0.03 + 0.0015\ (13.2)\ (1 - 0.03))$$

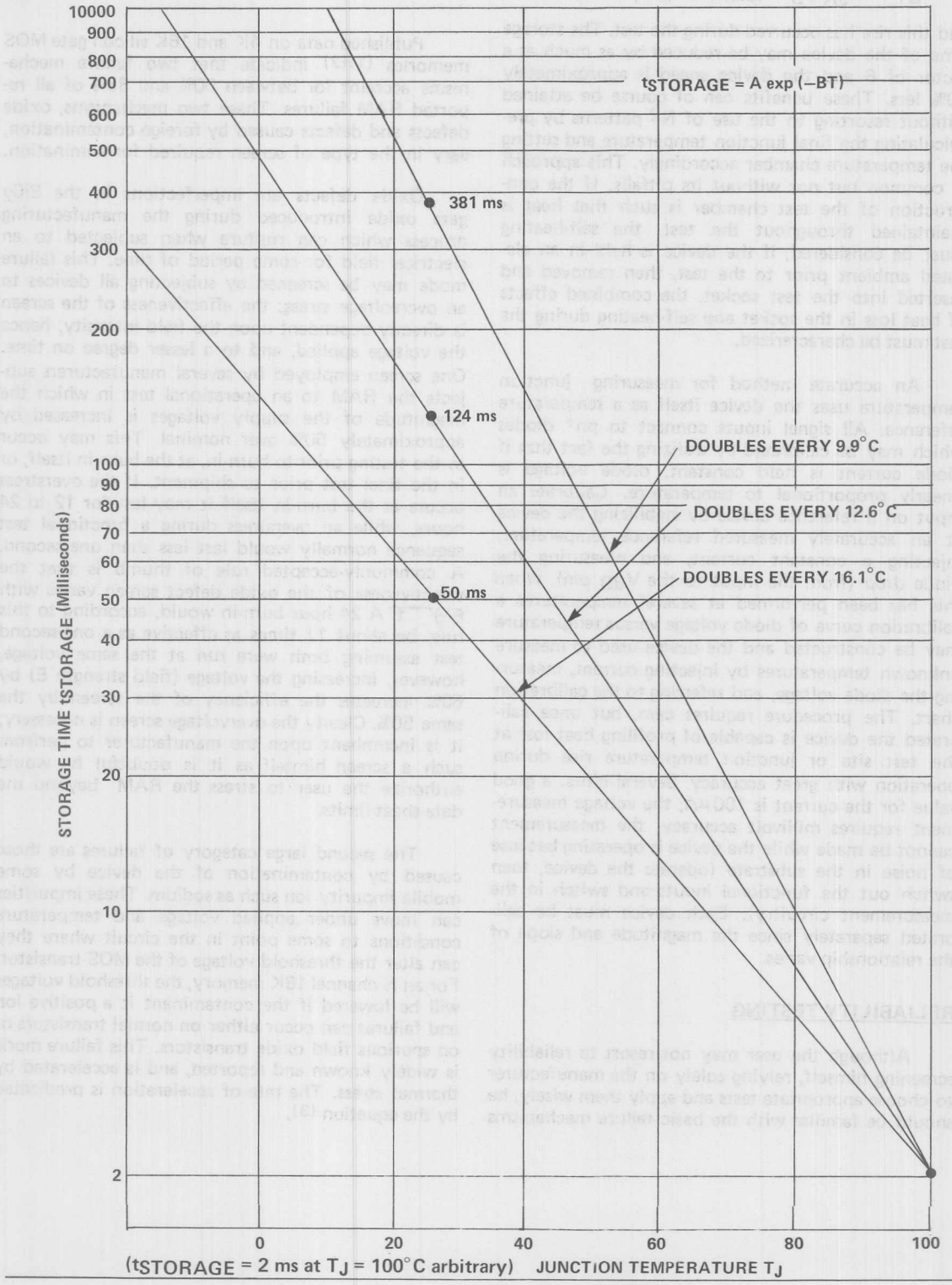
$$= 2.3^\circ\text{C}$$

The junction temperature of a device executing a 381 ms refresh test at T_A = 25 ° C would rise only 2.3 degrees to 27.3 °C, while the same device executing a 2ms refresh test at T_A = 70° C would have a junction temperature of 98°C.

Strictly speaking, the foregoing calculations are true only if the refresh test in question is run in a continuous mode allowing the junction temperature to stabilize. The thermal mass of the device is not negligible; in fact θ_{JA} is a function of time and has a time constant of approximately 60 seconds in most test situations. Much of the effectiveness of the N^2 test patterns can be attributed to higher junction temperatures due simply to the test length. An N^2 pattern, with N equal to 16384 and a cycle time of 375ns, requires 100 seconds. The value of θ_{JA} after 100 seconds of testing is about 80% of its final

STORAGE TIME VS JUNCTION TEMPERATURE

Figure 1



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value. The junction rise for P_D = 462 milliwatts is

$$\Delta T = \theta_{JA} P_D = (0.8)\ (70^\circ C/W)\ (.462) = 26^\circ C$$

and this rise has occurred during the test. The storage time of the device may be reduced by as much as a factor of 6 and the device speed is approximately 10% less. These benefits can of course be attained without resorting to the use of N^2 patterns by precalculating the final junction temperature and setting the temperature chamber accordingly. This approach is common but not without its pitfalls. If the construction of the test chamber is such that heat is maintained throughout the test, the self-heating must be considered; if the device is held in an elevated ambient prior to the test, then removed and inserted into the test socket, the combined effects of heat loss in the socket and self-heating during the test must be characterized.

An accurate method for measuring junction temperature uses the device itself as a temperature reference. All signal inputs connect to pn^+ diodes which may be calibrated by utilizing the fact that if diode current is held constant, diode voltage is linearly proportional to temperature. Calibrate an input on a reference device by stabilizing the device at an accurately measured reference temperature, injecting a constant current, and measuring the diode drop (from the input to the V_{BB} pin). When this has been performed at several temperatures a calibration curve of diode voltage versus temperature may be constructed and the device used to measure unknown temperatures by injecting current, measuring the diode voltage, and referring to the calibration chart. The procedure requires care, but once calibrated the device is capable of profiling heat loss at the test site or junction temperature rise during operation with great accuracy. Several hints: a good value for the current is 100 μA; the voltage measurement requires millivolt accuracy; the measurement cannot be made while the device is operating because of noise in the substrate (operate the device, then switch out the functional inputs and switch in the measurement circuitry). Each device must be calibrated separately since the magnitude and slope of the relationship varies.

RELIABILITY TESTING

Although the user may not resort to reliability screening himself, relying solely on the manufacturer to choose appropriate tests and apply them wisely, he should be familiar with the basic failure mechanisms and methods employed to screen them out prior to shipment.

Published data on 4K and 16K silicon gate MOS memories [1][2] indicate that two failure mechanisms account for between 50% and 85% of all reported RAM failures. These two mechanisms, oxide defects and defects caused by foreign contamination, vary in the type of screen required for elimination.

Oxide defects are imperfections in the SiO_2 gate oxide introduced during the manufacturing process which can rupture when subjected to an electrical field for some period of time. This failure mode may be screened by subjecting all devices to an overvoltage stress; the effectiveness of the screen is directly dependent upon the field intensity, hence the voltage applied, and to a lesser degree on time. One screen employed by several manufacturers subjects the RAM to an operational test in which the magnitude of the supply voltages is increased by approximately 50% over nominal. This may occur in the testing prior to burn-in, at the burn-in itself, or in the final test prior to shipment. If the overstress occurs at the burn-in itself it may last for 12 to 24 hours, while an overstress during a functional test sequence normally would last less than one second. A commonly-accepted rule of thumb is that the effectiveness of the oxide defect screen varies with $E\sqrt{t}$. A 24 hour burn-in would, according to this rule, be about 17 times as effective as a one-second test assuming both were run at the same voltage, however, increasing the voltage (field strength E) by 50% increases the efficiency of the screen by the same 50%. Clearly the overvoltage screen is necessary; it is incumbent upon the manufacturer to perfrom such a screen himself as it is doubtful he would authorize the user to stress the RAM beyond the data-sheet limits.

The second large category of failures are those caused by contamination of the device by some mobile impurity ion such as sodium. These impurities can move under applied voltage and temperature conditions to some point in the circuit where they can alter the threshold voltage of the MOS transistor. For an N channel 16K memory, the threshold voltages will be lowered if the contaminant is a positive ion and failures can occur either on normal transistors or on spurious field oxide transistors. This failure mode is widely known and reported, and is accelerated by thermal stress. The rate of acceleration is predicated by the equation [3],

$$R = R_o \exp\left(-\frac{E_A}{KT_k}\right)$$

where

R is reaction rate

R_o is a constant

E_A is activation energy in electron volts (eV)

K is Boltzmann's constant (8.63×10^{-5} eV/°K)

T_k is temperature in degrees Kelvin (°K).

The activation energy for contamination-related failures is approximately 1.0 eV, and therefore such failures are subject to removal by high-temperature burn-in, and most manufacturers perform an operating burn-in at 125°C for some number of hours (normally 12 - 24 hours) to reduce the incidence of field failures. On the other hand, the acceleration rate for for gate oxide failures is reported to be between 0.1 – .05 eV and the high-temperature screen would be marginally effective for gate oxide defects.

At least one manufacturer has combined the overvoltage and high temperature screens and is currently subjecting all 16K RAM's to a 24 hour burn-in at 125°C with the device power supplies at 50% overvoltage (+18 v, –7 v). Here again, such testing is properly done by the manufacturer, but the user should satisfy himself as to the adequacy of the reliability screens performed by the various manufacturers.

Reliability can be greatly impacted by proper design techniques. As an example, consider the equation given for thermal acceleration of failures. Rewriting the equation to allow a comparison of reaction rates at two different temperatures T_{k1} and T_{k2}, we have:

$$\frac{R_1}{R_2} = \exp\left(-\frac{E_A}{K}\left(\frac{T_{k2} - T_{k1}}{T_{k1}\,T_{k2}}\right)\right).$$

Now the effect of power dissipation upon reliability can be evaluated. For two 16K RAMS, one dissipating 900 milliwatts and one dissipating 450 milliwatts while operating at $T_A = 70°C$,

$$T_{J1} = 70°C + (70°C/W)\ (0.900\ W) = 133°C$$

$$T_{J2} = 70°C + (70°C/W)\ (0.450\ W) = 101.5°C$$

and assuming that $E_A = 1$ eV,

$$\frac{R_1}{R_2} = \exp\left(-\frac{1}{8.63 \times 10^{-5}}\left(\frac{133 - 101.5}{(133+273)(101.5+273)}\right)\right)$$

$$\frac{R_1}{R_2} = 0.097$$

which predicts a failure rate for the 900 milliwatt device of about 11 times that of the 450 milliwatt device, due to the 31.5° C difference in junction temperature.

MULTIPLEXED DEVICES

All 16K devices announced to date have followed the pinout and address multiplexed architecture pioneered by MOSTEK for their 4K RAM in 1973. The reduction in number of address lines from 14 to 7 (for the 16K) is bought at the expense of a more complex cycle with more timing parameters[4].

Some of these parameters must be examined in detail, as a proper understanding of their interrelationship is necessary. The timing diagram of Figure 2 shows the timing parameters necessary for standard write and read operations. The data output signal is shown for both the MOSTEK and Intel designs.

Three clocks, $\overline{RAS}$ (Row Address Strobe), $\overline{CAS}$ (Column Address Strobe) and $\overline{WRITE}$, must be provided along with seven multiplexed address lines and the D_{IN} (data in) if the memory is to execute a write cycle. Most of the testing difficulties arise from the relationship of $\overline{RAS}$ to $\overline{CAS}$, from the relationships of the addresses to $\overline{RAS}$ and $\overline{CAS}$, and from the relationships of the addresses to $\overline{RAS}$ and $\overline{CAS}$, and from $\overline{CAS}$ to the D_{OUT} (data output).

$\overline{RAS}$ initiates the cycle by going from the high state to the low state. It must have remained high long enough for internal nodes to be precharged to a known initial state prior to initiation of a new cycle; if the parameter t_{RP} is violated (made too short) internal clocks, address buffers, decoders, and sense amplifiers are not adequately initialized. Once $\overline{RAS}$ goes low it must remain low long enough (t_{RAS}) for the selection of the accessed cells, sense operation, and restoration of the destroyed data (the 1T cell reads out destructively). When $\overline{RAS}$ goes low it clocks in the seven row addresses if the row address setup and hold specifications (t_{ASR} and t_{RAH}) have been met. For the Intel design, if $\overline{CAS}$ is low when $\overline{RAS}$ goes low, a refresh-only operation is initiated; for the MOSTEK design, $\overline{CAS}$ may be low at the $\overline{RAS}$ transition (may in fact stay low for some time after the $\overline{RAS}$ transition since the parameter t_{CRP} is

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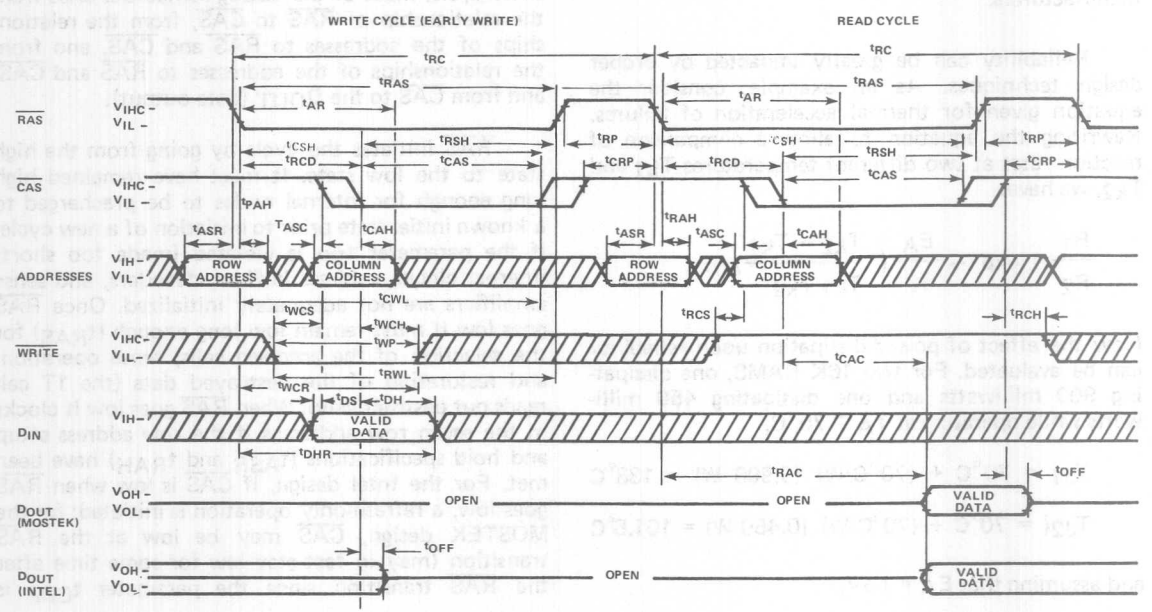
to perform a 64 cycle refresh hinges on this timing parameter. If $\overline{RAS}$ finds $\overline{CAS}$ low, the most significant row address bit along with all column address bits are ignored. This causes the selection of one row in each 8K half of the array and activation of all 256 sense amplifiers. Refresh may then be performed as though the array were organized as 64 rows by 256 columns. For the MOSTEK part, and for the Intel part if $\overline{RAS}$ finds $\overline{CAS}$ high, refresh must be performed on all 128 rows.

$\overline{CAS}$ is used to clock the column addresses, select one of the 128 active sense amplifiers and transfer its data to the output in a read or read/-write cycle. The high to low transition of $\overline{CAS}$ latches the column addresses if the column address setup and hold specifications (t_{ASC} and t_{CAH}) have been met. To prevent the $\overline{RAS}$ to $\overline{CAS}$ timing from intruding into the access time specification, 16K designs allow $\overline{CAS}$ to go active as soon as the row address hold time has been met and the column address is established on the address inputs. In fact, a negative specification on the column address setup allows switching $\overline{CAS}$ low even during the multiplex time. This negative specification becomes harder to meet as the part becomes faster (higher V_{DD}, lower seven address signals (with respect to $\overline{CAS}$) determines the actual value of t_{ASC}. Even though $\overline{CAS}$ can go negative at t_{RAH}, it is not required to do so until somewhat later in the cycle. The latest time for the $\overline{CAS}$ transition with respect to $\overline{RAS}$ is given by the parameter t_{RCD} (max) — note that t_{RCD} (min) equals the row address hold time t_{RAH}. The parameter t_{RCD} (max) is actually a pseudo-limitation, since the only effect of exceeding t_{RCD}(max) is to extend the access time specification (actually the row access) t_{RAC} by the actual value of t_{RCD} minus t_{RCD} (max).

Manufacturers are willing to live with the limitations posed by the negative value for column address setup time in order to provide a more usable part. The amount of time available to the user to switch his multiplexer without artificially delaying $\overline{CAS}$ and thereby degrading access time is simply the value of the maximum allowable $\overline{RAS}$ to $\overline{CAS}$ delay minus the required row address hold time, minus the required column address setup time (Multiplex time = t_{RCD} (max) — t_{RAH} —t_{ASC}). If t_{ASC} is a negative number it adds to rather than decreases the multiplex time. In order to guarantee this specification, the

TIMING DIAGRAM

Figure 2



KEY PARAMETERS OF CURRENTLY AVAILABLE 16K RAMS

Figure 3

MANUFACTURER	INTEL	MOSTEK
PART NUMBER	2116-2	4116-2
$\overline{RAS}$ ACCESS	200 ns	150 ns
$\overline{CAS}$ ACCESS	125 ns	100 ns
MULTIPLEX TIME	40 ns	40 ns
PRECHARGE TIME	75 ns	100 ns
NUMBER OF REFRESH CYCLES	64 or 128	128
NUMBER OF SENSE AMPS	256	128
DIE AREA	33930 mils^2	22330 mils^2
V_{DD} TOLERANCE	± 10%	± 10%
I_{DD} CURRENT (MAXIMUM)	69 mA	35 mA
POWER DISSIPATION (MAXIMUM)	911 mW	462 mW

III

manufacturer must place a minimum access time requirement on his testing – that is, parts which are too fast must be rejected, as they will not meet the negative t_{ASC} specification. It is to be expected that as faster 16K designs become available, this negative parameter will become smaller, or possibly will go to zero.

In addition to clocking the column addresses, $\overline{CAS}$ controls the state of the data output. The MOSTEK version open-circuits the output with the low to high transition of $\overline{CAS}$. Intel uses the high to low edge of $\overline{CAS}$ for the same purpose. This allows compatibility with the earlier 4K designs which also used the high to low edge of $\overline{CAS}$. The 4K's have, however, an extra chip select input which can be used in conjunction with $\overline{RAS}$ and $\overline{CAS}$ to deselect the output. With the Intel 16K the only way to guarantee a deselected output is to insert an extra cycle which leaves $\overline{RAS}$ high while clocking $\overline{CAS}$. MOSTEK overcomes this difficulty by unlatching the output with the rising edge of $\overline{CAS}$. This makes the output state independent of the previous cycle and eliminates the need for the "$\overline{CAS}$-only" deselect cycle. If the MOSTEK part is operated in a minimum cycle with $\overline{RAS}$ and $\overline{CAS}$ going high at the same time, the output is only valid for the deselect time (t_{OFF}) plus the amount that the speed of the actual device exceeds the specified speed (if any). To overcome this difficulty, MOSTEK allows the user to leave $\overline{CAS}$ low while $\overline{RAS}$ goes into precharge, thereby prolonging the output and, incidentally, adding the second major timing difference, that of the state of $\overline{CAS}$ when $\overline{RAS}$ goes low, which was discussed earlier.

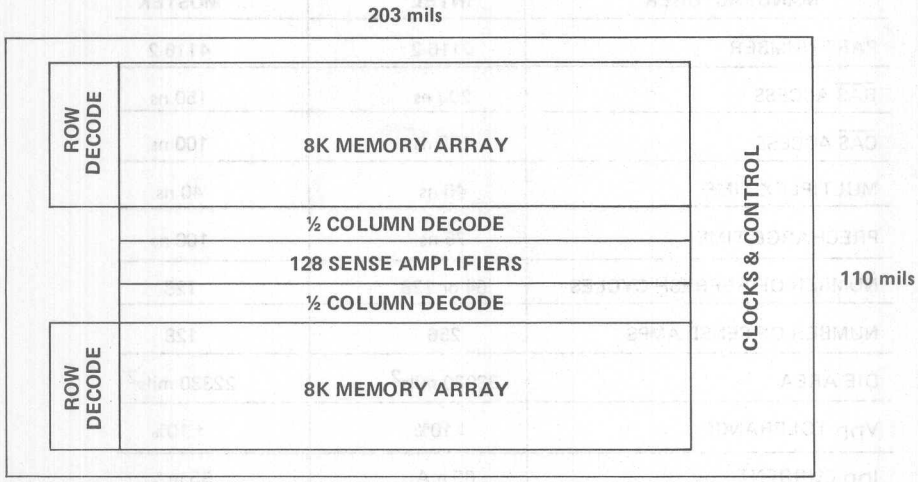
CHIP ARCHITECTURE AND CELL LAYOUT

The architecture of the chip can have a direct bearing on the types of tests which should be conducted, as can the layout of the storage cell. Precise details are difficult to acquire as most manufacturers consider them proprietary. Interest in the 16K has prompted the generation of several articles and papers which give some details useful in testing considerations[5][6][7]. Figure 4 gives a gross overview of two chip architectures which nevertheless provide some useful information.

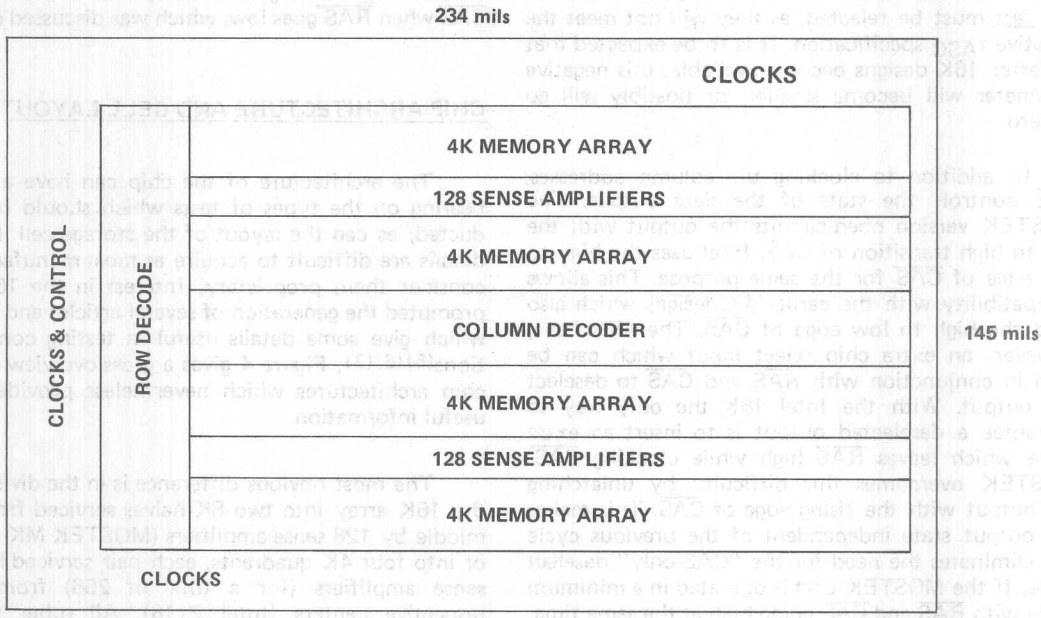
The most obvious difference is in the division of the 16K array into two 8K halves serviced from the middle by 128 sense amplifiers (MOSTEK MK 4116), or into four 4K quadrants, each pair serviced by 128 sense amplifiers (for a total of 256) from their respective centers (Intel 2116). All other factors being equal, in particular assuming approximately equal cell capacitances (reported by MOSTEK and Intel as 0.04 pF and 0.03 pF, respectively), the extra subdivision on the Intel chip means that the digit lines are only half as long as in the MOSTEK chip

TWO 16K RAM CHIP ARCHITECTURES

Figure 4



MOSTEK MK 4116



INTEL 2116

PROCESS COMPARISON
Figure 5

SINGLE LEVEL POLYSILICON GATE PROCESS FLOW	DOUBLE-LEVEL POLYSILICON GATE PROCESS FLOW
INITIAL OXIDE/NITRIDE	INITIAL OXIDE/NITRIDE
MASK 1 DEFINES ACTIVE AREA	MASK 1 DEFINES ACTIVE AREA
FIELD OXIDATION	FIELD OXIDATION
GATE OXIDATION	GATE OXIDATION
DEPOSIT POLYSILICON	DEPOSIT POLYSILICON
	MASK 2 DEFINES POLY I
	INSULATING OXIDE
	DEPOSIT POLYSILICON
MASK 2 DEFINES POLY	MASK 3 DEFINES POLY II
PHOSPHOROUS DIFFUSION	PHOSPHOROUS DIFFUSION
INSULATING OXIDE	INSULATING OXIDE
MASKS 3 & 4 DEFINE CONTACTS	MASKS 4 & 5 DEFINE CONTACTS
ALUMINUM	ALUMINUM
MASK 5 DEFINES METALLIZATION	MASK 6 DEFINES METALLIZATION
TOP GLASS	TOP GLASS
MASK 6 OPENS PAD AREAS	MASK 7 OPENS PAD AREAS

and, since signal varies with the ratio of digit line to cell capacitance, that the Intel sense amplifier should have twice the available signal as does the MOSTEK version. Since the digit line halves (or quarters) are precharged during the $\overline{RAS}$ inactive time (t_{RP}) to (hopefully) equal voltage, and since any difference in the starting values of the digit line voltages subtract directly from the available signal, MOSTEK may be rather more concerned about the precharge time than Intel, and, in fact, the value of t_{RP} for the MOSTEK 150 nanosecond part is specified to be 100 nanoseconds, while the t_{RP} value for the Intel 200 nanosecond part is actually smaller (75 nanoseconds).

On the other hand, the substrate (back of the chip) may be considered a noise collector which couples all areas of the circuit together. Since the clocks and decoders, prime noise generators, are strung along the short diminsion of both chips, a reasonable estimate of the substrate noise would be that it peaks in the center of the short axis, falling to zero toward the edges. The sense amplifiers in the MOSTEK design are located in the center and would presumably see a balanced noise coupling onto the digit lines, while the Intel sense amplifiers, located at the one quarter and three quarter points, might see more noise coupled onto the digit line quarters near the chip center than on the outer digit line quarters.

Since the sense amplifier naturally inverts one of the digit lines, it would be convenient if the test equipment made provision for exclusive - OR'ing either the most significant row address bit (for the MOSTEK design) or the second most significant row address bit (for the Intel design) with data into and out of the device under test such that a programmed input of all "ones" would be stored by the chip as all "highs". This facility would greatly simplify refresh and disturb tests. Of course, the sense amplifier inversion is logically removed by the chip itself so that it is transparent to the user, but the capability would be extremely useful in a test environment.

extension of the single-level polysilicon gate process common in the semi-conductor industry for years. Figure 5 is a basic comparison of the POLY II™ process as implemented by MOSTEK, and the standard single level poly process. There is only one additional mask required, plus one extra deposition and one extra oxidation step. Figure 6 depicts a cross-section through the cell and the cell schematic. The transfer gate (POLY II transistor) is used only in the cell; the threshold voltage for this transitor may be adjusted independently of the threshold voltage of the peripheral transistors. The ratio of digit line to cell capacitance is about 20:1 for the MOSTEK design and approximately 13:1 for the Intel.

MK4116 CELL AND CROSS–SECTION

Figure 6

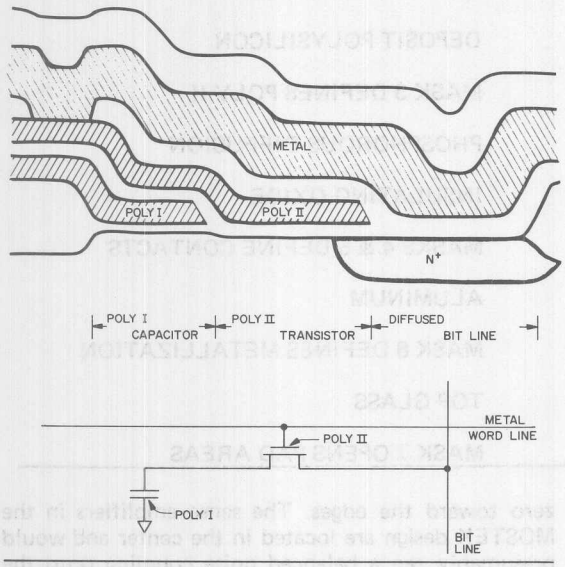


Figure 7 shows the cell layout which with minor variations, is used by both MOSTEK and Intel. The adjacent cells are located either on the same row or on rows separated by one word line and are always on adjacent columns. The first level polysilicon sheet which forms the common capacitor plate for all cells also forms the gate of an MOS field transistor which links neighboring cells. It may therefore be necessary to check for cell to cell interactions due to less than ideal field threshold voltage of this device. Also, the channel length of the transfer gate is determined by the relative alignment of first poly to second. If the misalignment is too great, the threshold voltage of the transfer gate may be reduced due to gate to the digit line.

TEST PATTERNS

The problem of developing test patterns to test memories for various pattern sensitivities has been extensively reported in the literature [8][9][10]. More recently, the emphasis has shifted towards analysis of the design and adoption of test sequences which exploit possible weaknesses [11]. This approach is necessary if test times for 16K RAM's are to be kept within practical bounds. The following information, although believed to be general, applies specifically to the MOSTEK design.

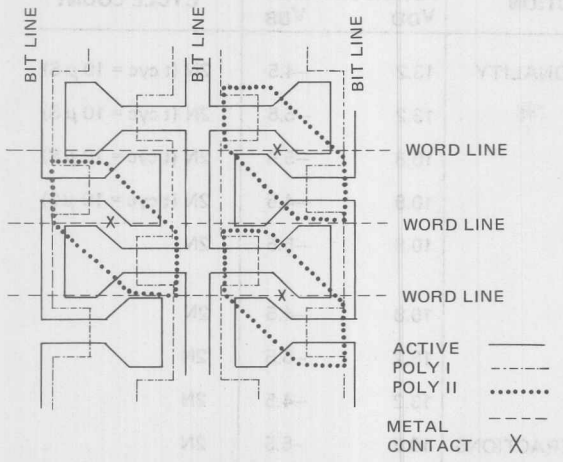
The 16K RAM is basically a synchronous machine built around a rectangular memory array, the coordinates of which are "rows" and "columns". The synchronous machine provides the timing control for the input latches, row decoder, sense amplifier, column decoder, write circuitry, and output latch. In contrast to earlier, asynchronous RAM's, the 16K nearly always fails digitally. That is, if a problem exists with the input latches, the wrong output will be generated (but not a "late" output which is correct but delayed by, for example, poor input levels). There is no "worst-case" pattern for access time since access time is controlled by the internal clock generators. This greatly simplifies the testing of gross functionality, which must only assure cell uniqueness and output validity over the specified timing and power supply ranges.

On the other hand, the memory array and sense amplifiers must still be checked for pattern sensitivities. Considering the signal detection capabilities of the sense amplifier, and its precharge requirements, a probable "worst-case" pattern for a sense amplifier is a single bit of DATA in a field of $\overline{\text{DATA}}$. If such a pattern is run in a "row fast" mode, each sense amplifier will be required to perform some number of reads of $\overline{\text{DATA}}$, a single detection of DATA, and complete the scan reading $\overline{\text{DATA}}$. If the DATA bit occupies, at some time, each of the locations along the digit line, the ability of the sense amplifier to pick signal out of noise and to remove completely any influence of the preceding cycles on the present cycle will have been checked. Note that this pattern would require only as many scans as there are bits per

sense amplifier, and that all columns can be checked simultaneously.

MK4116 CELL LAYOUT

Figure 7



Considering the row select function, noise coupling considerations indicate that here too a worst case pattern might be either a single DATA bit in a field of $\overline{DATA}$, or, perhaps, a solid field. Here also the word "field" has a restricted meaning, applying only to all cells connected to a single row select line.

Several patterns check for the above failure modes efficiently; one of particular interest is the $2N^{3/2}$ "Moving Diagonal" pattern, which requires 128 write-read scans through the entire array. On the first scan, all bits are written to $\overline{DATA}$ with the exception of the 128 bits along the major diagonal which are written to DATA. The read scan verifies the correct operation of the array under these conditions. On each succeeding scan, the position of the diagonal of DATA is shifted until, on the 128 scan, it has occupied every possible position in the array. Each cell has once been the only DATA cell in a row and column of $\overline{DATA}$. This pattern has proven to be quite effective in screening the 16K RAM.

Refresh tests can be separated into two categories: still and dynamic. Still refresh tests are performed by writing all locations, pausing for the refresh interval with $\overline{RAS}$ and $\overline{CAS}$ inactive (high), and reading all cells. The inactive pause allows the cells to leak low but also allows internal nodes which are bootstrapped above V_{DD} by the trailing edge of $\overline{RAS}$ or $\overline{CAS}$ to decay so that both the cells and the dynamic periphery are tested. Unfortunately, such a test normally is not worst case for the cell, as noise generated during active cycles can contribute to the loss of data in the cell. The dynamic refresh tests write data into some subset of cell (normally half of the cells) and, during the refresh interval, perform either read or write cycles on the cells not being tested, the intent being to couple charge-degrading noise onto the unaccessed test cells. Both tests are necessary to completely guarantee functionality of the 16K.

During the active portion of a cycle, 127 of the 128 rows are not selected, and must remain at OFF to prevent partial selection of a transfer gate. A test with maximum active time provides greatest opportunity for such partial selection to occur. This test might perform a write scan with minimum precharge times (t_{RP}) and maximum active time (t_{RAS}), followed by a read-modify-write scan under the same basic timing conditions, followed by a read scan to verify the "modify-write" operation. This important test is often overlooked but is in fact worst-case for many of the internal circuits.

For users desiring a basic but adequate test sequence, the above patterns provide a good starting point. Figure 8 summarizes such a sequence which should provide a reasonable degree of confidence in any RAM which passed. Special timing modes and certain timing parameters would be left unchecked, but could be easily added if desired. This test sequence requires $(28N + 4N^{3/2})$ cycles, of which all but 8N may be at the fastest allowable cycle rate. The 8N are at the slowest allowable cycle rate (maximum cycle length). If the cycle times are 375 nanoseconds and 10 microseconds, respectively, this sequence would execute in just over 4.5 seconds, exclusive of tester overhead and power supply settling times.

III

POSSIBLE MINIMUM TEST SEQUENCE FOR 16K RAM

Figure 8

TEST DESCRIPTION	DATA PATTERN	FUNCTION	POWER SUPPLIES V_{DD}	V_{BB}	CYCLE COUNT
MAXIMUM CYCLE	DIAGONAL	FUNCTIONALITY	13.2	–4.5	2N (t cyc = 10 μS)
	$\overline{\text{DIAGONAL}}$		13.2	–5.5	2N (t cyc = 10 μS)
	DIAGONAL		10.8	–5.5	2N (t cyc = 10 μS)
	$\overline{\text{DIAGONAL}}$		10.8	–4.5	2N (t cyc = 10 μS)
LOAD READ	PARITY and $\overline{\text{PARITY}}$		10.8	–5.5	2N
			10.8	–4.5	2N
			13.2	–5.5	2N
			13.2	–4.5	2N
LOAD READ	CHECKERBOARD and $\overline{\text{CHECKERBOARD}}$	BIT INTERACTIONS	10.8	–5.5	2N
			10.8	–4.5	2N
			13.2	–5.5	2N
			13.2	–4.5	2N
MOVING DIAGONAL	DIAGONAL	FUNCTIONALITY	10.8	–5.5	$2N^{3/2}$
			13.2	–4.5	$2N^{3/2}$
DYNAMIC REFRESH	ALTERNATE ROWS	DATA RETENTION	10.8	–5.5	1N + 2 mS
DYNAMIC REFRESH	$\overline{\text{ALTERNATE ROWS}}$	DATA RETENTION	10.8	–5.5	1N + 2 mS
STILL REFRESH	ALL HIGHS	DATA RETENTION	10.8	–5.5	2N + 2 mS

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TEST IMPLICATIONS OF HIGHER SPEED 16K RAMS

Testing

As the delivery of a new generation of 16K dynamic MOS random access memories reaches higher volume stages, new and more complex problems are confronting both the device test engineer and the test equipment manufacturer. Economically feasible solutions to many of the problems will require the adoption of new and sometimes controversial philosophies regarding memory testing. Certainly a more thorough characterization and knowledge of each device type is required in order to insure adequate testing within reasonable test time limits.

TESTING PROBLEMS

Probably the most obvious problem associated with testing 16K RAMs is that of test times. Since many commonly used pattern sensitivity tests vary in length as a function of the number of bits in the memory (N) by a factor of $N^{3/2}$ or N^2, test time considerations for production testing of 16K RAMs can be quite significant. The following table illustrates the test time penalties paid in moving from 4K RAM testing to 16K RAMs:

TEST TIMES FOR VARIOUS TEST PATTERNS
(CYCLE RATE = 375ns)

	N=4096	N=16384
2N(load-read)	3ms	12ms
$2N^{3/2}$(moving pattern, row or column Ping-Pong)	197ms	1.6sec.
$2N^2$(Ping-Pong GALPAT)	12.6sec.	201sec.

The test times listed assume only one pass testing. Testing at multiple voltage corners, timing sets, temperatures, etc. will increase the test times listed for each pattern accordingly.

A second problem which is aggravated by higher speed specifications for 16K RAMs is that timing accuracies on presently available memory test equipment are often not adequate to test particular timing specifications. For example, higher speed 16K RAM specifications call for a row address setup time specification of 0ns and a row address hold time specification of 15ns relative to the row address strobe input. For a tester specified at ±1ns accuracy on any timing edge from the programmed value including internal clock skews, cables, driver, and transition times, the actual value of a row address hold time programmed to be 15ns could be as little as 13ns or as much as 17ns and still be within the tester specification. Since the actual device speed distribution for this parameter may be less than 10ns wide, a ±2ns tester accuracy could result in significant correlation problems between testers if an attempt were made to specify and test this parameter to the actual device capabilities.

A potentially more severe problem affecting 16K RAM test correlation is power supply, input, and output noise during functional testing. Power dissipation on 16K dynamic RAMs is dynamic in nature with power supply current transients sometimes in excess of 100ma occurring synchronously with internal device clock edges charging and discharging the capactive loads of internal circuit nodes. As seen in Figure 1, the rise and fall times of these current transients can sometimes be as short as 10ns. Because of these transients, it is extremely important that proper power supply decoupling techniques be used

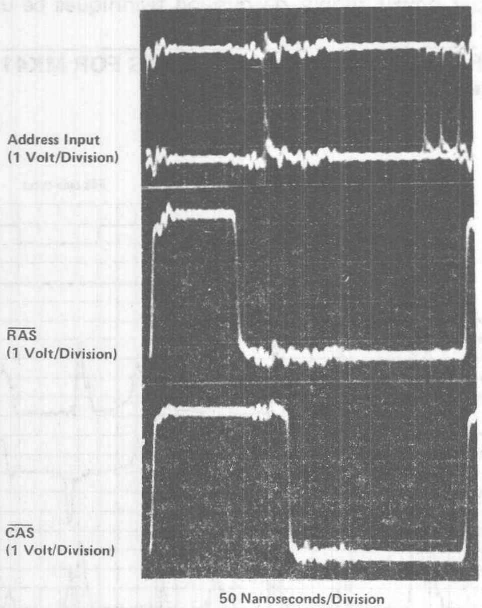
TYPICAL CURRENT WAVEFORMS FOR MK4116
Figure 1

to insure relatively "clean" signals at the device during functional testing. However, even with extensive engineering precautions it is sometimes impractical to achieve less than two or three hundred millivolts of peak-to-peak noise on power supply and signal inputs at the device during functional testing especially when a temperature controlled handler is also involved. Temperature controlled handlers usually complicate the problem of minimizing inductance and decoupling power supplies as near to the device as possible and therefore can add significantly to the magnitude of noise at the device.

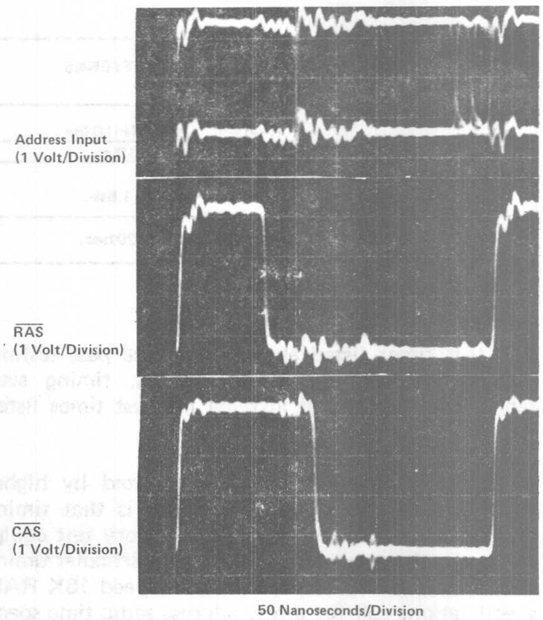
Figures 2 and 3 are examples of the relative integrity of the input signals measured at the device during functional testing of a 16K RAM with the device under the test being physically located first at the test head and then at the end of the handler interface connections. For the example shown, the total lead length for each handler interface signal connection including contactor is approximately 2 inches.

The effects of noise during functional testing vary depending on device type and test conditions. However, in general, noise problems become more severe transients on the power supplies increase in magnitude and thus induce more noise than slower devices. Also the "windows" during which data is sampled become shorter on faster devices enabling noise of short durations to have a more severe effect. For example, consider a previous generation 4K RAM with a minimum specified access time of 250ns and a minimum address valid time of 60ns versus a new generation 16K RAM with a minimum specified access time of 120ns and a minimum address valid time of 15ns. The 250ns 4K RAM typically requires that the addresses be valid for a minimum of 30ns in order to interpret the address data correctly. However, on the faster 16K RAM design, in order to allow more time for system address multiplexing, a circuit was developed capable of interpreting valid addresses in less than 5ns. For the 4K RAM the effects of a noise transient of a 5ns duration on an address input during the valid address sampling time would probably be insignificant since it's magnitude would be integrated over a 30ns period but for the 16K RAM the effects of the same noise transient during it's address sampling time would obviously be much more significant. Noise transients should not cause failures in 16K RAM operation unless the peak voltages of the transients violate the specified dc opera-

16K RAM INPUT TEST SIGNALS AT TEST HEAD
Figure 2



16K RAM INPUT TEST SIGNALS AT TEST SITE OF TEMPERATURE HANDLER
Figure 3



effect on the operation of 16K RAMs in the system specified to operate with an input logic "0" level of 0.8 volts maximum. However, under "worst case" test conditions with the dc logic "0" input level set at 0.8 volts, transients of even smaller magnitudes can cause device failures resulting in tester correlation problems.

As 16K RAM designs continue to achieve higher performance goals, the problems of distinguishing device failures versus failures induced by noise transients or timing inaccuracies of the test equipment are reaching a new order of significance. Attempts to do "worst case" testing of all specified device parameters simultaneously will usually result in the failure of some quantity of devices that actually, will meet specifications. In many cases a thorough characterization of the device design and process to be utilized can eliminate the need for 100% testing for all specified limits and conditions.

CHARACTERIZATION

The success of any characterization and resulting economically feasible production test program for a particular 16K RAM device type is highly dependent upon the RAM design. If the device is marginal and subject to complex pattern, data, temperature, or voltage sensitivities the development of a comprehensive and economically practical production test procedure could prove to be impossible. Unlike previous 1K and 4K RAM designs, deficiencies such as N^2 pattern sensitivities cannot be tolerated in 16K RAMs. When proper techniques are utilized, it is possible for 16K dynamic RAMs to be designed so that sensitivities due to process variations and weaknesses can be detected using relatively simple and economical address and data pattern test sequences.

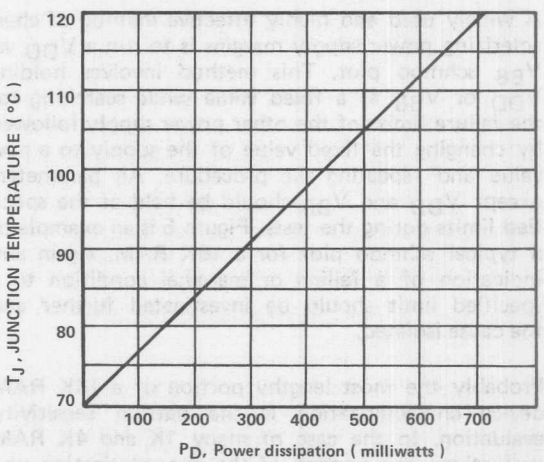
The goal of a 16K RAM device characterization should be to identify any sensitivities of the particular 16K RAM design over the full production range of process parameters and the resulting production tests required that are comprehensive in screening for device sensitivities, optimized in terms of test time and economics, and operate within the constraints of the available test equipment. One of the first and most important steps in such a characterization is the selection of the sample to be analyzed. The sample should be large enough to contain a variety of process weaknesses and cover several different fabrication weeks to allow for a maximum of process parameter variation. For some tests such as timing and input voltage parameter characterization, a few hundred devices are probably sufficient, but for other tests such as pattern characterization where that particular device characteristics do not change over a period of time, it is advisable to periodically repeat portions of the characterization sequence.

Since virtually all characterization tests will be repeated at the specified temperature extremes for the device, the junction temperature at which each device should be tested in order to guarantee the specified maximum ambient temperature for that device type should be first determined. Most 16K RAMs are specified over the temperature range 0°C to 70°C ambient. The junction temperature (T_J) of each device depends on the power dissipation (P_D) of that device by the equation:

$$T_J = T_A + P_D \theta JAX$$

θJAX is the thermal impedance between the device junction and system ambient. Figure 4 is a graph of this equation for θ JAX = 70°C per watt which is standard for a 16 pin ceramic dual-in-line package. In order to calculate the proper junction test temperature for a 70°C ambient, the power dissipation on a sample of 16K RAMs must be measured operating continuously at an ambient temperature of 70°C and at the maximum specified frequency.

JUNCTION TEMPERATURE VS. POWER DISSIPATION FOR T_A =70°C
Figure 4



If the device junction temperature is stabilized by using a long warm-up period at the maximum specified operating frequency prior to the first test, the proper test temperature is the specified maximum ambient temperature. If the test is only a few seconds long, then the junction temperature will rise during test only by a few degrees and the proper test temperature should be nearer to the calculated value for junction temperature.

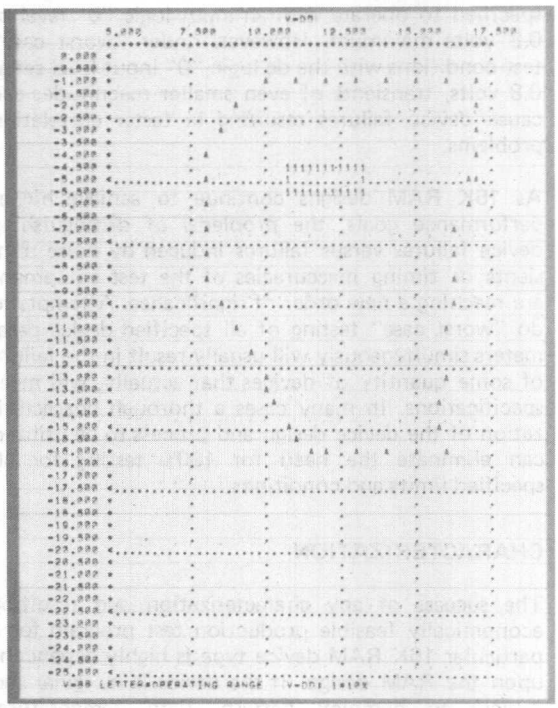
The first stages of the characterization tests should include an extensive analysis of the voltage, power dissipation, and timing characteristics and margins of the device. The test patterns used for these tests will generally be very simple such as a load-read checkerboard or diagonal pattern. For input voltage and timing testing, each device should first be tested at the specified limits for all parameters at the four voltage corner extremes of V_{DD} and V_{BB}. V_{CC} margin testing is usually not necessary since this power supply is connected only to the device output. Each input timing and voltage parameter should then be varied separately until a failure occurs, recording the last passing value of the parameter being tested. If during these tests any parameter evaluated appears to fail or be marginal to a specified limit, then the reason for this condition should be further evaluated with the cause being isolated to a design process or tester fault. A typical example of this type of condition for a 16K RAM might be an indication from the initial characterization data that the maximum input zero level specification of 0.9 volts on the address inputs is marginal when in fact further investigation isolates the problem to noise on the address inputs at the device during the times at which the row and column addresses were being strobed into the device. In this case it would be necessary to correct the problem on the test equipment or compensate the input zero voltage level so that the data from further characterization tests would not be erroneously influenced.

A widely used and highly effective method of characterizing power supply margins is to run a V_{DD} vs. V_{BB} schmoo plot. This method involves holding V_{DD} or V_{BB} at a fixed value while searching for the failure limits of the other power supply followed by changing the fixed value of the supply to a new value and repeating the procedure. All parameters except V_{DD} and V_{BB} should be held at the specified limits during the tests. Figure 5 is an example of a typical schmoo plot for a 16K RAM. Again any indication of a failing or marginal condition to a specified limit should be investigated further and the cause isolated.

Probably the most lengthy portion of a 16K RAM device characterization is the pattern sensitivity evaluation. In the case of many 1K and 4K RAM evaluations this portion of the characterization was not completed. Instead lengthy pattern sensitivity tests were inserted into production test programs with the hope that these tests would be effective in screening for any pattern sensitivities that might exist. This philosophy can obviously not be economically applied to 16K RAM testing.

A thorough 16K RAM pattern sensitivity characterization should include a variety of pattern tests designed to screen for different types of failure

V_{DD} VS. V_{BB} SCHMOO PLOT FOR 16K DYNAMIC RAM
Figure 5



modes and sensitivities of RAMs. These tests are usually referred to by names such as load-read, address complement, march, active refresh, still refresh, walking columns, walking diagonal, galloping rows, galloping columns, write disturb, surround disturb, column disturb, and galpat. It is usually sufficient to run most of the pattern tests at maximum specified frequency but a sample of patterns such as march, address complement, and walking diagonal should also be run at the slowest specified cycle rates. Each device in the characterization sample should be screened for pattern sensitivities at the four (4) corners of the V_{DD} and V_{BB} power supplies and at the specified temperature extremes. The test procedure should be such that all test patterns are tried on each device regardless of previous test pattern failures for the device under test with the test conditions recorded on all failures. Because of test time constraints it should be sufficient to run the longer N^2 pattern tests such as galpat on a sample of a few hundred devices covering a wide range of process parameters, while screening a larger sample of devices to the remaining pattern tests. By analyzing the data gathered from the test described, it should be possible to define a set of test patterns and conditions that is optimal in terms of test time without sacrificing test integrity. The result of an optimized test flow is that pattern tests

are run only at the power supply voltage corners that have been identified as "worst case" for that pattern, and lengthy pattern sensitivity tests are utilized only when the device sensitivities that these patterns detect cannot be identified using shorter test patterns.

When sensitivities of a device to lengthy test pattern sequences are discovered, it is often possible to develop alternate test methods and patterns that result in dramatically reduced test times and are designed specifically to screen for device related failure modes. The development of such a procedure usually requires that the failure mechanism be well understood in relation to the particular device design.

A successful example of a test procedure developed to screen for a particular device sensitivity is presently being used in the production testing of one 4K RAM device. During the characterization of this device a sensitivity to a disturb type of pattern was discovered. The pattern used consisted of writing the full memory with "1's" followed by writing a "0" two thousand times at the base location. The entire memory, excluding the base cell, was then read checking for an all "1's" pattern. The base location was then written to a "1" and the entire procedure repeated with the base cell incrementing through all possible memory locations. Assuming a 500ns cycle rate, the test time for this sequence was greater than 20 seconds. Initial investigation of the problem revealed that after each base cell had been written 2000 times it was necessary to read only the column of the base location instead of the entire array in order to generate the failure mechanism, which reduced the test time to 4 seconds. Upon further investigation it was found that the failures were caused by voltages slightly in excess of the device threshold voltage being coupled onto the row select line connected to the gates of the one transistor storage cells for that row. Since the base cell on the failing column was repeatedly being written to a "0" causing the column digit bus to be low each cycle, the voltage coupled onto the failing row was sufficient to cause the stored "1" level on the failing cell to be discharged through the cell transistor somewhat each cycle. When enough disturb cycles had occurred to discharge the cell sufficiently, the failure resulted. Since the failure mechanism is highly dependent on the threshold voltage of the cell transistor which varies as a function of the V_{BB} supply voltage, it was possible to reduce the number of disturb write cycles of the base location required from 2000 to 100 cycles by implementing the test at a V_{BB} supply voltage 0.5 volts more positive than the specification normally allows, further reducing the test time requirement to approximately 200 milliseconds. In order to prevent an unnecessary yield loss due to the abnormal supply voltage conditions, a relaxation of the input "0" voltage level was required for the test.

PRODUCTION-TESTING

Once the initial 16K RAM device characterization is completed enough data concerning the characteristics and sensitivities of the particular design should be available to establish a logical and comprehensive production test sequence. Since single temperature production testing is economically desirable, the characterization data must be analyzed for the feasibility of insuring that all devices' specifications are met over the entire operating temperating range for the device while testing at a single temperature. The high temperature extreme virtually always proves to be the only practical choice for a single test temperature because of refresh and parameter margin characteristics of 16K dynamic RAMs. The "worst case" condition for pattern sensitivities power supply margins and timing parameters is typically at high temperatures, but the lower temperature limits can be "worst case" for some device parameters such as input levels and power dissipation. For the device parameters that prove to be the "worst case" at the lower temperature extreme, it should be possible to determine the proper guardbands to be used for high temperature testing from the characterization data.

An important factor which is too often not thoroughly comprehended in establishing the production test conditions for high performance 16K dynamic RAMs is the characteristics and limitations of the production test equipment to be utilized. As discussed previously, tester timing skews of as little as ±1ns can be significant and cause severe correlation problems considering the large number of critical input timing specifications relative to the clock inputs for 16K RAMs. Because of variables such as internal tester clocks, skews, cables to remote temperature handlers, and individual driver characteristics, controlling input timing skews to a tighter specification often proves to be impractical. Fortunately, however, for most 16K dynamic RAM designs, virtually all critical input timing parameters track the column access time of the device as a relatively constant percentage, and by analyzing the device characterization data a correlation factor for each input timing parameter relative to column access time can usually be established. Since the specified column access times, even for higher performance 16K dynamic RAMs, is a relatively large value (typically 90ns or greater), a ±2ns maximum total measurement error is of much less significance. Therefore for most 16K RAM designs, testing for the proper column access times on each device and relaxing the programmed test conditions on input timing signals by a few nanoseconds so that even "worst case" tester timing skews will not violate the specified device limits is sufficient to guarantee that all device timing specifications are met without causing severe tester correlation problems.

cult test equipment related problems to be addressed in 16K dynamic RAM testing. The maximum effort practical should be extended to insure that the integrity of the signals applied to the device under test are the best possible, but often even this does not prevent noise related tester correlation problems. For most 16K dynamic RAMs, test equipment noise related failures occur when noise transients on the input signals at the device during functional testing exceed the "worst case" specified input logic level voltages for that device. Unless the noise levels are excessive, relaxing the programmed dc input voltage levels usually eliminates most failures of this type, but may not be desirable if input voltage level specifications for the device are to be guaranteed. Even though it is not always possible to eliminate noise related device failures when testing for "worst case" input voltage levels, it is possible to separate potential noise related failures by running a portion of the test patterns for each V_{BB} and V_{DD} power supply voltage corner tested at relaxed dc input levels and then change the input voltage levels to the specified "worst levels tests and then fail when the specification dc limits are applied can be placed through the test program software into a separate physical bin. Devices in this bin would then require further analysis in order to determine if the failures were device or noise related.

CONCLUSION

In order to establish test conditions for higher speed 16K dynamic RAMs that are effective and economical, the particular characteristics and sensitivities of both the device and production test equipment to be utilized must be understood. Test flows that are optimized for the particular characteristics of a 16K RAM design can result in dramatic savings in production testing costs without sacrifices in test integrity. However, economic success of an optimized 16K dynamic RAM test flow depends upon performing a thorough and lengthy device characterization and the choice of a design that is not sensitive to a wide variety of complex test conditions.

MOSTEK®

AN IN-DEPTH LOOK AT THE MK4027

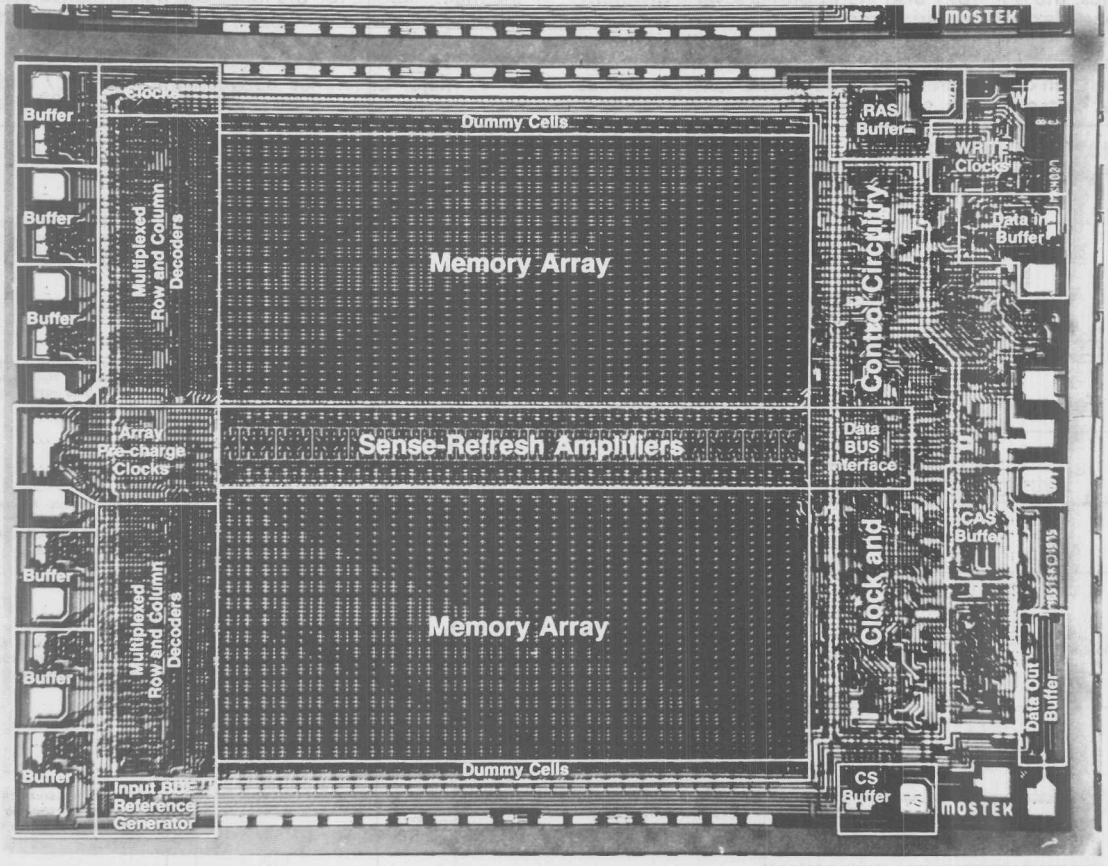
Application Note

The MK 4027, like its predecessor the MK 4096, is a 4096 word by 1 bit N-Channel MOS Random Access Memory circuit that is packaged in a standard 16-pin DIP. This small package size is the result of a unique multiplexing and latching technique for the address inputs which MOSTEK pioneered for its 4K RAM family. This innovative approach to dynamic RAM design has proven to be one of the most important semiconductor memory milestones in the past few years. With more than a dozen manufacturers having announced their intentions to produce equivalent circuits with identical pin configurations, the MOSTEK 16-pin 4K RAM family has become an industry standard.

The purpose of this application note is to acquaint the user with the MK 4027, and to provide a more complete and in-depth understanding of the circuit (and its use) than can be obtained from the data sheet alone. MOSTEK realizes that most experienced memory system designers go through a process of evaluating many potential memory devices and making a judgement as to which device is best for a particular application. MOSTEK also realizes that this evaluation process can be a very tedious and time consuming endeavor, especially if several potential candidates are to be evaluated. Therefore, the information presented in this application note is divided into major sections and presented in the order that MOSTEK has found to be most desirable in the typical evaluation process used by most designers.

III

Figure 1

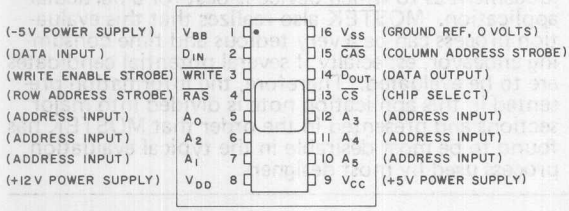


BACKGROUND

The pin configuration for the 16-pin 4K RAM was originated by MOSTEK Corporation when the MK 4096 was announced in 1973. Basically, the 16 pin device is made possible by eliminating six of the twelve address inputs required to select one out of 4096 bit locations in the RAM. Addressing is accomplished by the external generation of negative going Row and Column Address Strobe signals ($\overline{RAS}$ and $\overline{CAS}$) which latch incoming multiplexed addresses into the chip. This same addressing technique is carried over from the MK 4096 to the higher performance MK 4027.

PIN CONNECTIONS

Figure 2



In addition to improved performance characteristics, the MK 4027 also incorporates several different and flexible operating modes and system-oriented features. These features include direct interfacing capability with TTL, low capacitance inputs and output, on-chip address and data registers, two methods of chip selection, simplified ($\overline{RAS}$-only) refresh operation, and flexible column address timing to compensate for system timing skews. Also, the MK4027 offers a unique cycling operation called page-mode. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

Before delving into the more detailed aspects of the MK 4027, it is helpful to obtain a basic understanding of the internal circuit operation. Once a designer understands the fundamental operation of the MK 4027, it is much easier to see how and why the device operates with such improved performance over existing 4K dynamic RAM designs.

Much of the internal structure of the MK 4027 is made possible by state-of-the-art processing. The MK 4027 is fabricated with MOSTEK's ion-implanted N-Channel silicon gate (Poly I) process, whose basic steps are illustrated in figure 3. This process allows independent adjustment of gate and field oxide thresholds by ion-implantation (a technique introduced by MOSTEK in 1971), which maximizes performance, density, and reliability.

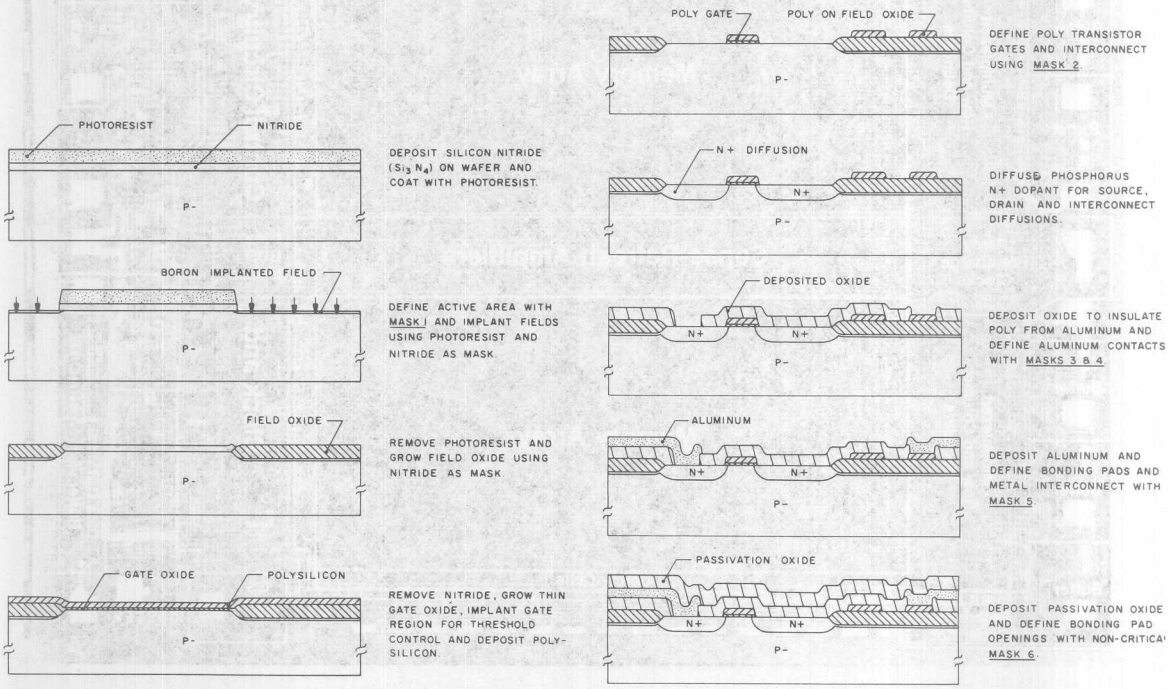
INTERNAL CIRCUIT OPERATION

The internal circuit operation of the MK 4027 is unlike any other 4K RAM in the industry. The MK 4027 utilizes a revolutionary new architecture for semiconductor memories. The circuit layout and design techniques incorporated within the MK 4027 are the main reasons for the increased performance capabilities and the additional system-oriented features. As an aid in understanding the operation of the MK 4027 refer to the block diagram in figure 4.

A major difference between the MK 4027 and most conventional RAMs is that the MK 4027 has

4027 PROCESS STEPS

Figure 3



only one internal decoder and only one set of input buffers for both the Row and Column addresses. This feature greatly reduces the active silicon area and input capacitance. Note also that the internal single transistor storage cell matrix is divided into two sections with the sense amplifiers and input/output circuitry located between the two. This type of sense amp configuration causes data stored in half of the memory to be inverted from the data stored in the opposite half. However, this inversion is completely invisible at the device terminals. The sense amplifiers incorporated within the MK 4027 are dynamic, balanced, differential sense amps which dissipate no D C or steady-state power. Furthermore, virtually all of the circuitry used in the MK 4027 is dynamic and consequently, most of the power dissipated by the MK 4027 is a function of operating frequency rather than active duty cycle.

MEMORY CYCLES

The MK 4027 will begin a memory cycle as soon as the Row Address Strobe ($\overline{RAS}$) input is activated. This is done by changing the voltage potential at the $\overline{RAS}$ input from a high level to a low level. The first internal action that takes place is the conversion of the TTL-compatible $\overline{RAS}$ signal to the MOS (12 volt) level that is required within the chip. The internal amplifier that performs this conversion is, of necessity, powered up at all times. Therefore, the $\overline{RAS}$ input buffer always dissipates some D C power. The steady-state power dissipated by the $\overline{RAS}$ input buffer is the main component of the overall standby power.

After the Row strobe reaches the proper level internally, a series of internal clock edges are generated to perform special control functions. The first of these clocks serves as a signal to "trap" the first set of six addresses into the address input buffers. These input buffers then generate the address into both true and complement form in high level, as required by the decoder. The addresses are then decoded for selection of the proper row in the memory cell matrix. Also, as the selected row is enabled, a set of dummy cells are enabled on the opposite side of the sense amplifier from the selected Row. These dummy cells serve to establish the proper trip point or reference voltage as required by the sense amps to differentiate between a one level and a zero level when the selected cell is read. As the selected Row and dummy cells are enabled, the address input buffers are already being reset and precharged so that the column addresses can be multiplexed into the chip.

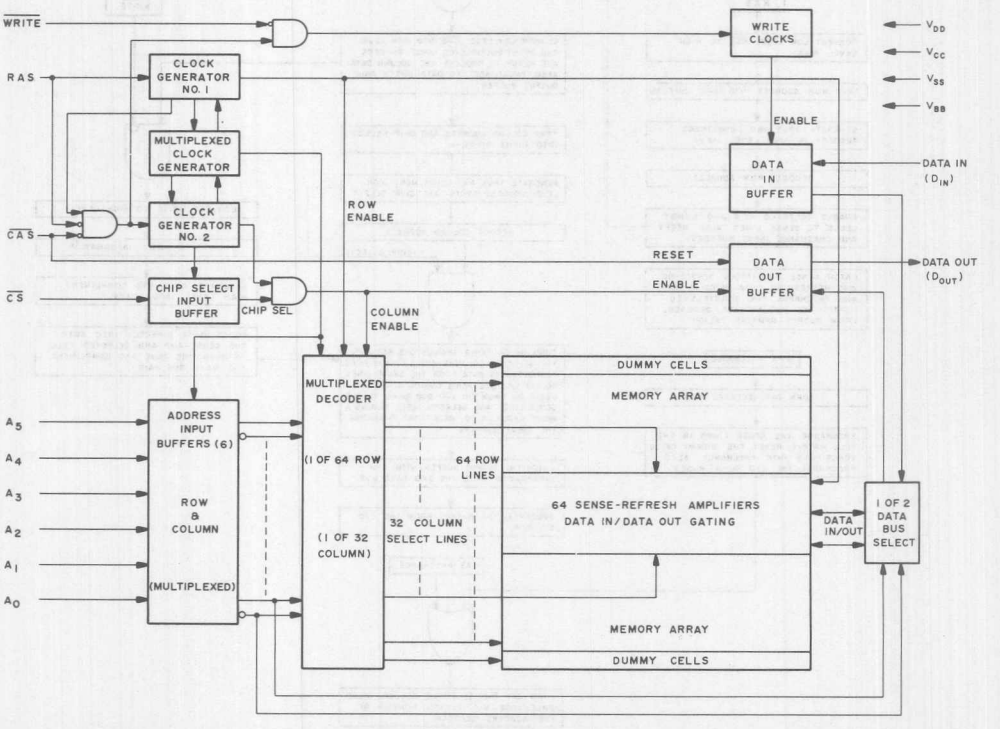
The last action initiated by the row clocks causes the data in all 64 cell locations in the selected Row to be latched into the sense amplifiers which , in turn, restore proper data back into the cells. (This action is known as refreshing.) The selected Row output from the decoder remains enabled as long as the Row Address Strobe ($\overline{RAS}$) is at a logic 0 level.

The second chain of events within the MK 4027 memory cycle, assuming that $\overline{RAS}$ is active, occurs when the Column Address Strobe ($\overline{CAS}$) is activated. As soon as the $\overline{CAS}$ is brought to logic 0 level, the output buffer is turned off and the output assumes the high impedance (open-circuit) state. If , at this time, the input circuitry is ready to process the column data, the low level $\overline{CAS}$ signal is converted to

III

MK 4027 FUNCTIONAL BLOCK DIAGRAM

Figure 4



a signal from the row clock generator. This signal inhibits all column clocks until the sequence of row clocks has progressed to the appropriate time in the memory cycle. The internal "gating" of the RAS and CAS clocks has a very significant impact on external operation of the part. This is discussed in detail in a later section of this application note.

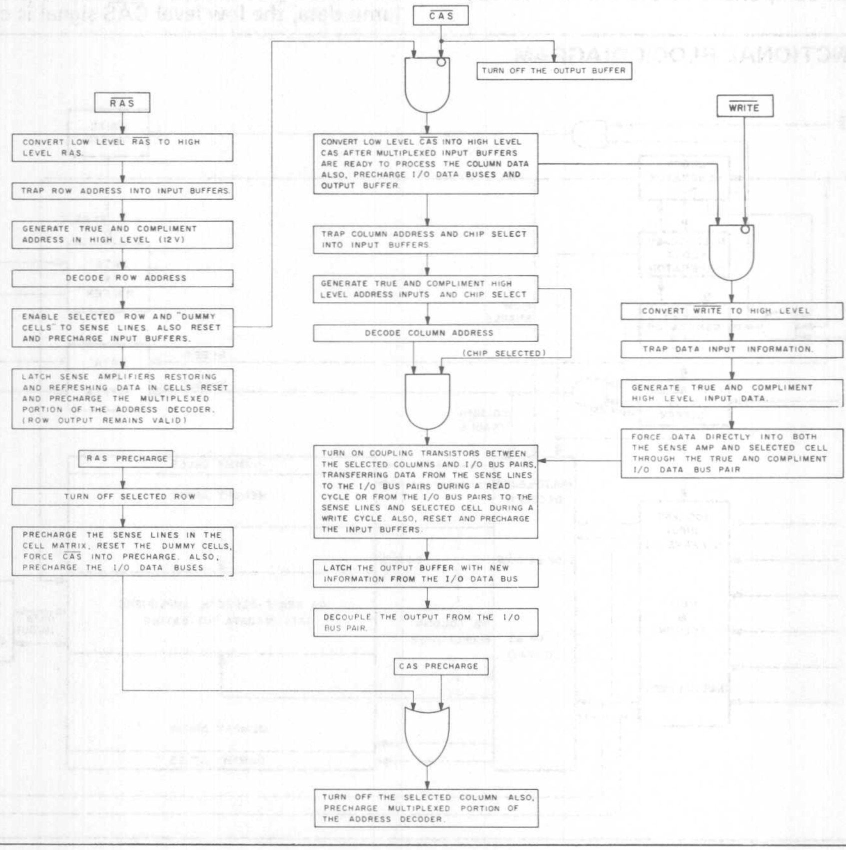
After CAS reaches the proper internal level, a series of clock edges are generated which operate in a similiar manner to the RAS clocks. In the case of CAS, however, the second rather than the first clock serves to "trap" the second set of six addresses into the address input buffers. These buffers again generate true and complement high level addresses as required by the decoder. Also, at this time the $\overline{\text{WRITE}}$ circuitry is enabled and the input/output data buses, which are routed through the center of the cell matrix, and the output buffer are all precharged to proper levels.

If the $\overline{\text{WRITE}}$ input is activated, a parallel series of clocks are enabled in addition to those enabled by the $\overline{\text{CAS}}$ circuitry alone. While the column addresses level information. It should be pointed out that the CAS circuitry also enables the Chip Select ($\overline{\text{CS}}$) input. The Chip Select input buffer is essentially the same type of circuit as an address input buffer, but, if the Chip Select input is not activated, the remaining series of CAS clocks are inhibited.

If, at this point in time, the chip has received a Row Address Strobe and a Column Address Strobe (with the Chip Select active), the chip will initiate either the Read or Write operation as indicated by the state of the $\overline{\text{WRITE}}$ input. The decoder selects the proper column by enabling the coupling transistors which connect the selected columns to the data input/data output differential bus pairs. During a read cycle, data is transferred from the selected sense lines to the I/0 bus pairs. A write cycle will cause data to be transferred from the selected data I/0 bus to the sense lines so that proper data is forced into the selected storage cell. After the correct data is present on the I/0 bus, the data output buffer is latched and the correct information is presented at the output of the chip. Once the output buffer is latched, the output is decoupled from the internal I/0 bus.

FUNCTIONAL FLOW CHART

Figure 5



After the chip has performed all the functions required for a read, write or refresh operation, it remains in a quiescent state until the input control clocks ($\overline{RAS}$ and $\overline{CAS}$) are taken to the inactive (high) state. If $\overline{RAS}$ remains active and $\overline{CAS}$ is taken to the precharge (high) condition, the previously selected column will be turned off and the multiplexed portion of the address decoder will be reset and precharged, ready for a new $\overline{CAS}$ cycle. However, the previously selected row will remain enabled and the sense amps will retain the information read from that row. (This feature of the MK 4027 makes possible "page-mode" operation.) When $\overline{RAS}$ is terminated, the selected Row is turned off, the sense lines and the data I/0 buses are precharged and the dummy cells are reset. Also, the input buffers and decoders are reset and precharged, ready for a new $\overline{RAS}$ cycle. Deactivating $\overline{RAS}$ also forces $\overline{CAS}$ into the precharge condition internally, even though $\overline{CAS}$ may remain active at the input.

The internal workings of the MK 4027 can be best summarized by referring to the Functional Flow Chart in figure 5. From this brief outline of the internal operation of the device it is easy to see how the MK 4027 is capable of so many different and flexible timing modes. Besides the usual read, write, and read-modify-write cycles, the MK 4027 is also capable of "page-mode" cycles (very useful in Direct Memory Access operation) and "delayed-write" cycles (very useful in shift register applications.) While keeping in mind the internal structure of the MK 4027 it is now appropriate to delve into a more detailed discussion of the external characteristics and system implications of the MK 4027 memory device.

EXTERNAL DEVICE CHARACTERISTICS

ADDRESSING

As stated earlier, the 12 address bits required to decode one of the 4096 cell locations within the MK 4027 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative-going, TTL-level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. Each of these clock signals, $\overline{RAS}$ and $\overline{CAS}$, triggers off a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" features allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the 6 address inputs have been changed from Row address to Column address information. This results in a system limit of $t_{RCD} = t_{RAH} + t_T + t_{ASC}$ (t_T = one transition time).

Note that $\overline{CAS}$ can be activated at any time after t_{RAH} and it will have no affect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end points result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to MK 4027 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time for $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

The significance of this "gated $\overline{CAS}$" feature is that it allows a multiplexed circuit, such as the MK 4027, to be comparable in performance (access time) with non-multiplexed devices such as the 18- and 22-pin 4K RAMs. In essence, it allows the designer to compensate for system timing skews that may be encountered in the multiplexing operation when addressing the device. In the MK 4027, the "window" available for multiplexing from row address to column address information while still achieving minimum access time (t_{RAC}) is a full 25% of access time.

MEMORY CYCLES

Once the MK 4027 is properly addressed, the device is capable of performing various types of memory cycles. Selection of the various cycles, whether read, write or some combination thereof, is controlled by a combination of $\overline{CAS}$ and $\overline{WRITE}$, while $\overline{RAS}$ is active. Also, since Chip Select ($\overline{CS}$) does not have to be valid until $\overline{CAS}$, which is well into the memory cycle, it is possible to start a cycle before it is known which is the selected device.

Data is retrieved from the memory in a read-only cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of these signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data-In register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed in by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the data input is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ goes low. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. Note that delaying $\overline{WRITE}$ until after the negative edge of $\overline{CAS}$ is termed a "read-write cycle" rather than read-modify-write. In a read-write cycle, it is not necessary to wait until data is valid at the output before the write operation is started. This feature is very useful when the MK 4027 is used in sequential memory applications or in systems that employ "interleaving techniques." However, if a true read-modify-write cycle is required (where the write operation occurs after read access), then $\overline{WRITE}$ can occur while $\overline{RAS}$ and $\overline{CAS}$ are still active and after t_{CAC}.

To take full advantage of this $\overline{CAS}/\overline{WRITE}$ signal relationship it is necessary for one to understand how the Data Out Latch is controlled. The most important fact to remember is that any change in the condition of the Data Out Latch is initiated by the $\overline{CAS}$ negative edge. The output buffer is not affected by memory cycles in which only the $\overline{RAS}$ signal is applied to the MK 4027. Whenever $\overline{CAS}$ makes a negative transition, the output will go unconditionally open-

circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then at access time the output latch and buffer will contain the input data. Once having gone active, the output will remain valid until the MK 4027 receives the next $\overline{CAS}$ negative edge. Intervening refresh cycles in which $\overline{RAS}$ is received, but no $\overline{CAS}$, will not cause valid data to be affected. Conversely, the output will assume the open-circuited state during any cycle in which the MK 4027 receives a $\overline{CAS}$ but no $\overline{RAS}$ signal (regardless of the state of any other inputs). The output will also assume the open-circuit state in normal cycles if the chip is unselected. Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} (Ground) for a logic 0. The effective resistance to V_{CC} (logic "1" state) is 420Ω maximum and < 100 Ω typically. The resistance to V_{SS} (logic "0" state) is 125Ω maximum and < 50Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the positive supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4027 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

Specified on the MK 4027 data sheet are two electrical characteristics of the device which guarantee the appropriate state of the data output during a write cycle. These two specifications, $\overline{RAS}$ to $\overline{WRITE}$ delay (t_{RWD}) and $\overline{CAS}$ to $\overline{WRITE}$ delay (t_{CWD}) are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. The values listed in the "minimum" and "maximum"

THESE PARAMETERS APPLY TO ALL MK 4027 MEMORY CYCLES:

SYMBOL	DEFINITION
t_{RFSH}	Maximum time that the device will retain stored data without being refreshed.
t_{RP}	$\overline{RAS}$ precharge, or $\overline{RAS}$ inactive time of a cycle.
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ lead time. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
t_{ASR}	Row address set-up time.
t_{RAH}	Row address hold time.
t_{ASC}	Column address set-up time.
t_{CAH}	Column address hold time.
t_{CSH}	Column address strobe hold time
t_{AR}	Column address hold time referenced to $\overline{RAS}$.
t_{CSC}	Chip select set-up time.
t_{CH}	Chip select hold time.
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$.
t_{CRP}	$\overline{CAS}$ inactive to $\overline{RAS}$ active precharge time.
t_{OFF}	Output buffer turn-off delay.
t_{RAS}	$\overline{RAS}$ pulse width or active time.
t_{CAS}	$\overline{CAS}$ pulse width or active time.
t_{RAC}	Access time from $\overline{RAS}$ falling edge.
t_{CAC}	Access time from $\overline{CAS}$ falling edge.
t_T	Transition time (rise and fall). Transition times are measured between V_{IHC} or V_{IH} and V_{IL}. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

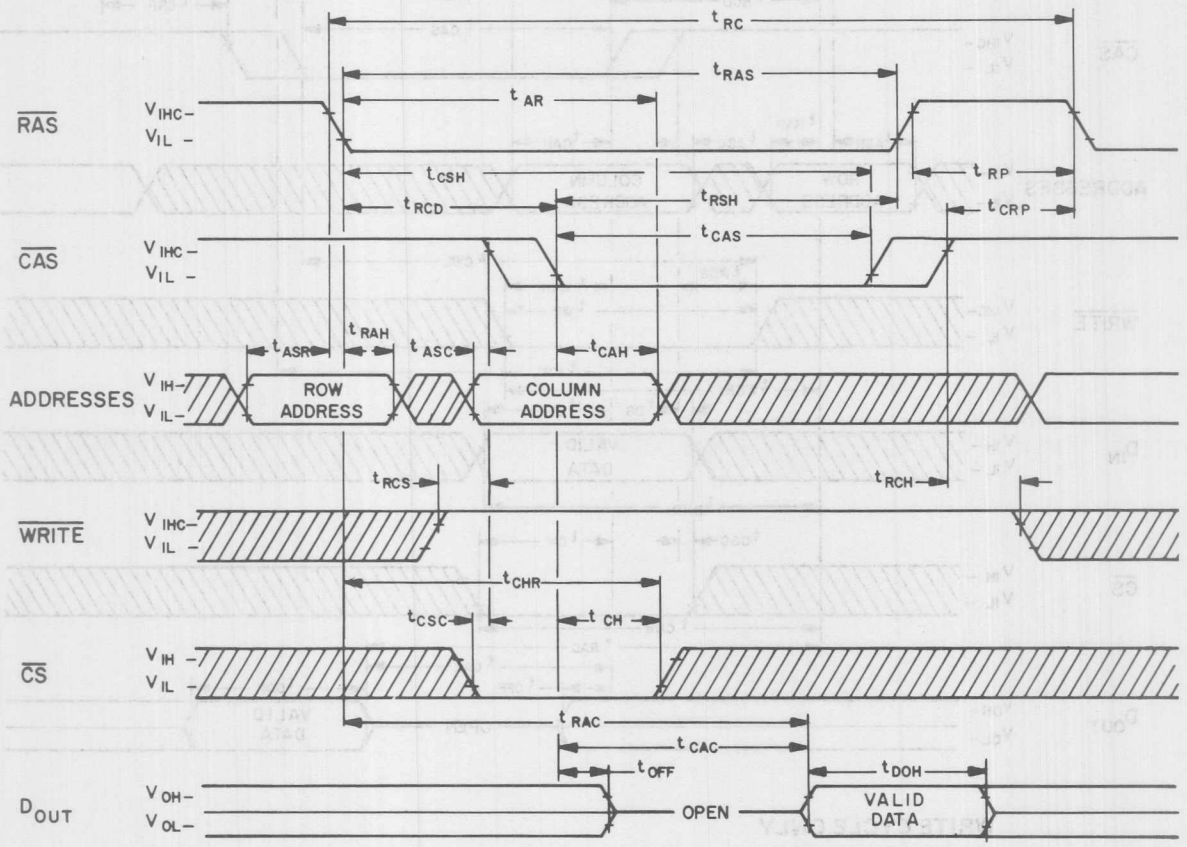
columns should be inserted as terms in the following equations:

1. If $t_{CWD} + t_T \leq t_{CWD}$ (min), the data out latch will contain the data written into the selected cell.
2. If $t_{CWD} \geq t_{CWD}$ (max) + t_T and $t_{RWD} \geq t_{RWD}$ (max) + t_T, the data out latch will contain the data read from the selected cell.
3. If t_{CWD} does not meet the above constraints then the data out latch will contain indeterminate data at access time.

The following diagrams are representations of the MK 4027 timing waveforms for read, write and delayed-write or read-modify-write cycles. A list of the timing parameters associated with each cycle is also included.

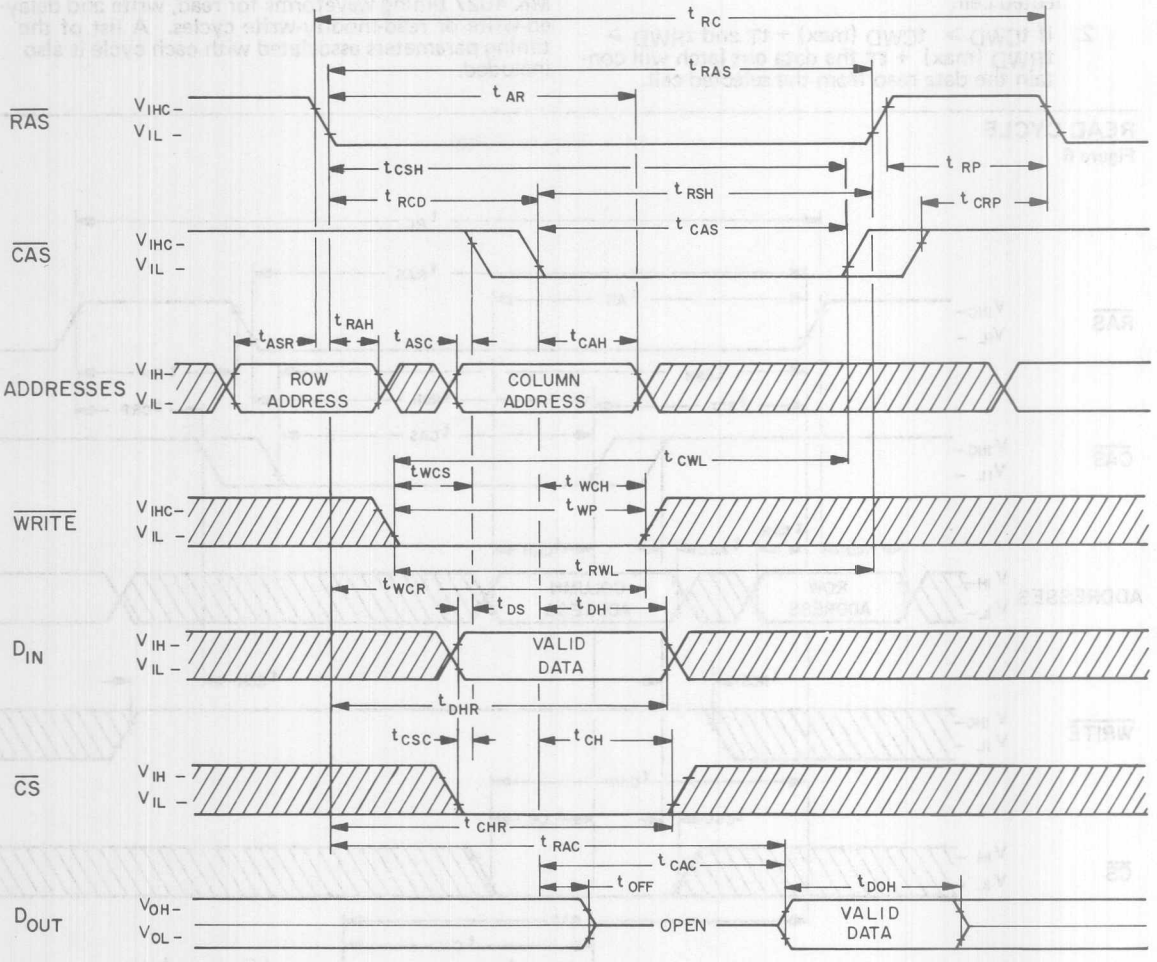
READ CYCLE

Figure 6



READ CYCLE ONLY

t_{RC}	Random read or write cycle time. t_{RC} (min) $\geq t_T + t_{RAS} + t_T + t_{RP}$.
t_{RCS}	Read command set-up time.
t_{RCH}	Read command hold time.
t_{ACC}*	Device access time, t_{ACC}, is the longer of two calculated intervals: 1. $t_{ACC} = t_{RAC}$, or 2. $t_{ACC} = t_{RCD} + t_T + t_{CAC}$ * This parameter is not shown in the timing waveforms.

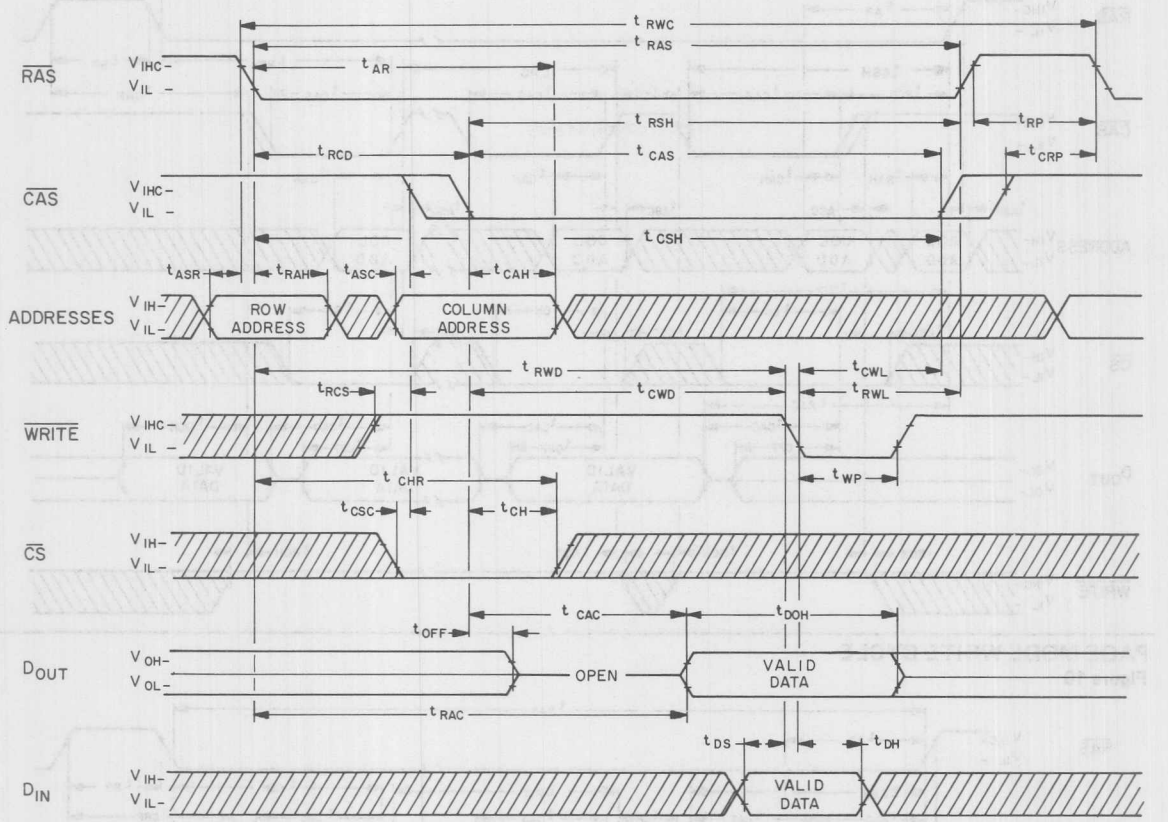


WRITE CYCLE ONLY

t_{RC}	Random read or write cycle time. t_{RC} (min) $\geq t_T + t_{RAS} + t_T + t_{RP}$.
t_{WCH}	Write command hold time referenced to $\overline{CAS}$.
t_{WCR}	Write command hold time referenced to $\overline{RAS}$.
t_{WP}	Write command pulse width.
t_{RWL}	Write command to $\overline{RAS}$ lead time.
t_{CWL}	Write command to $\overline{CAS}$ lead time.
t_{DS}	Data In set-up time (referenced to $\overline{CAS}$).
t_{DH}	Data In hold time (referenced to $\overline{CAS}$)
t_{DHR}	Data In hold time (referenced to $\overline{RAS}$)

READ - WRITE / READ - MODIFY - WRITE CYCLE

Figure 8



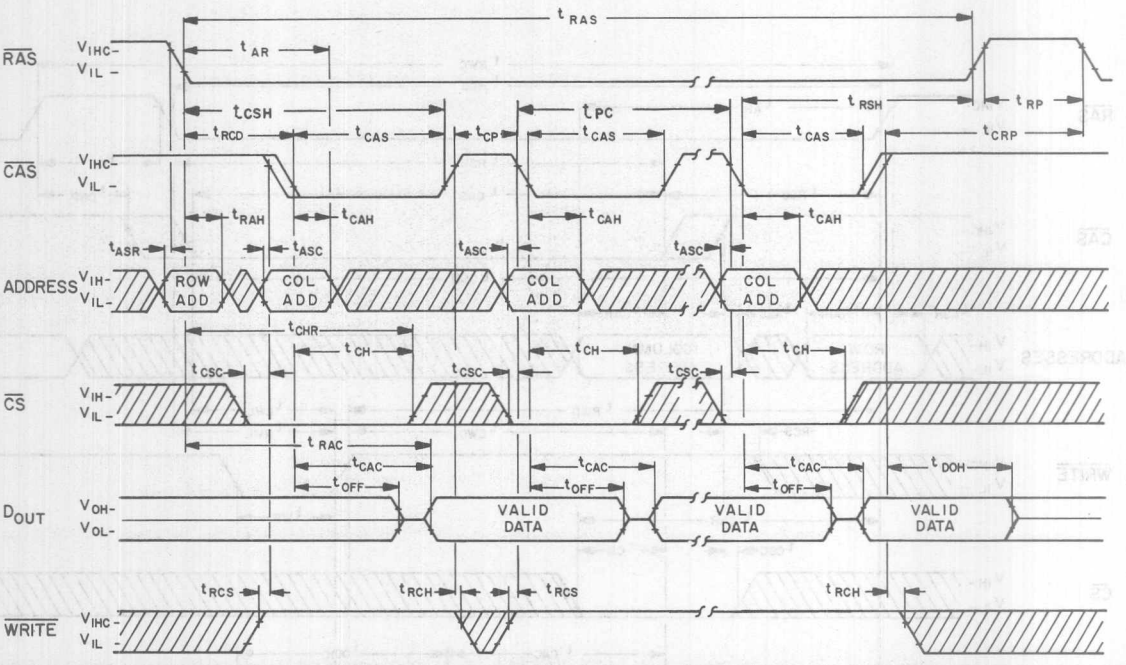
READ/WRITE CYCLE

t_{RWC}	Read-write or "delayed write" cycle time. t_{RWC} (min) $\geq t_T + t_{RCD} + t_T + T_{CWD} + t_{RWL} + t_T + t_{RP}$. This is the minimum time to insure that both a read and write operation will occur at the same address in a single memory cycle.
t_{RCS}	Read command set-up time.
t_{WP}	Write command pulse width.
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay.
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay.
t_{RWL}	Write command to $\overline{RAS}$ lead time.
t_{CWL}	Write command to $\overline{CAS}$ lead time.
t_{DS}	Data In set-up time (referenced to $\overline{WRITE}$).
t_{DH}	Data In hold time (referenced to $\overline{WRITE}$).

III

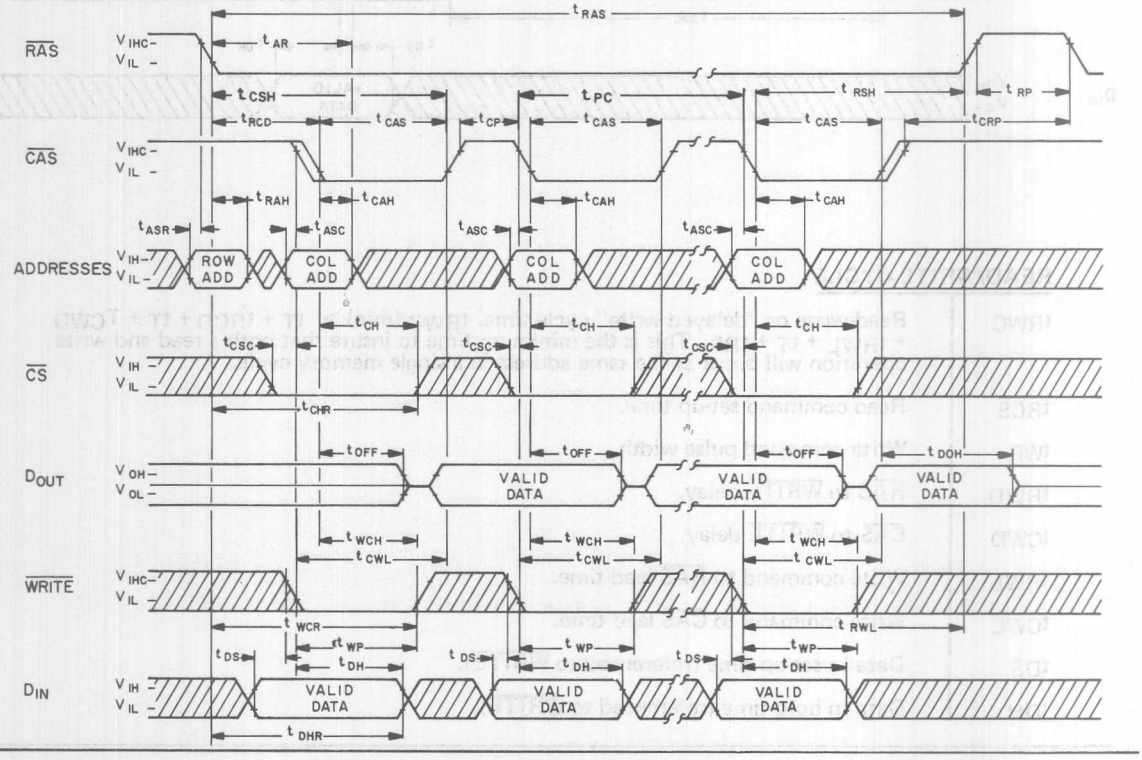
PAGE MODE READ CYCLE

Figure 9



PAGE MODE WRITE CYCLE

Figure 10



PAGE MODE

Keeping in mind the above mentioned cycle operations, it is now appropriate to introduce another category of memory cycles. The "page-mode" operation allows for successive memory operations at multiple column locations at the same row address with increased speed and with decreased power. This is done by strobing the row address into the chip and keeping the $\overline{RAS}$ signal active (at a logic 0) throughout all successive memory cycles in which the row address is common. This "page-mode" operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. Every type of cycle-read, write, read-modify-write and delayed-write cycles-can all be performed in the page mode. Also, the chip select ($\overline{CS}$) is operative in page mode just as in normal cycles. It is not necessary that the chip be selected during the first cycle for subsequent cycles to be selected properly in a page operation. Likewise, the $\overline{CS}$ input can be used to select or disable any cycle (s) in a series of "page" cycles. This feature allows the page boundary to be extended beyond the 64 column locations in a single chip. The page boundary can be extended by applying $\overline{RAS}$ to multiple 4K memory blocks and decoding $\overline{CS}$ to select the proper block.

The addition of page mode to the MK 4027's repertoire of features adds only two additional constraints to the timing parameters mentioned earlier. The first constraint is that the length of time that a single chip can remain in the page mode is limited to the maximum $\overline{RAS}$ pulse width (t_{RAS}) as specified on the data sheet. Second, the $\overline{CAS}$ precharge time (t_{CP}), or the time from the positive edge of $\overline{CAS}$ in one page cycle to the negative edge of $\overline{CAS}$ in subsequent page cycles must be obeyed.

The following timing waveforms illustrate the page mode operation. Note that the page-mode write cycle depicts the Data In set-up and hold times referenced to $\overline{WRITE}$ rather than $\overline{CAS}$. Once again, this is to illustrate the flexibility of the write cycle operation. Page-mode operation is particularly useful in transferring large blocks of data into or out of memory.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a $\overline{RAS}$ signal occurs, accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select ($\overline{CS}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell. If during a refresh cycle, the MK 4027 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. Therefore, data from the previous cycle will remain valid throughout the refresh cycle. However, if "$\overline{RAS}$-only" refresh cycles (where $\overline{RAS}$ is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. The output buffer will regain activity with the first cycle in which $\overline{CAS}$ is applied to the chip.

The following diagram illustrates the "$\overline{RAS}$-only" refresh cycle:

POWER DISSIPATION

The worst case power dissipation of the MK 4027, continuously operating at the fastest cycle rate, is the sum of [V_{DD} (max) X I_{DD} (max) plus V_{BB} (max) X I_{BB} (max)], where maximum currents are the maximum currents averaged over one memory cycle. The worst case power for the MK 4027 with a cycle rate of 375 nanoseconds is less than 470mW, while the typical power is 170 mW at a 1 μs cycle time.

Typical power supply current waveforms for various types of memory cycles are shown in figure 12. From this picture it is easy to see that most of the power drawn by the MK 4027 is the result of an address strobe charging the capacitances of various internal circuit nodes.

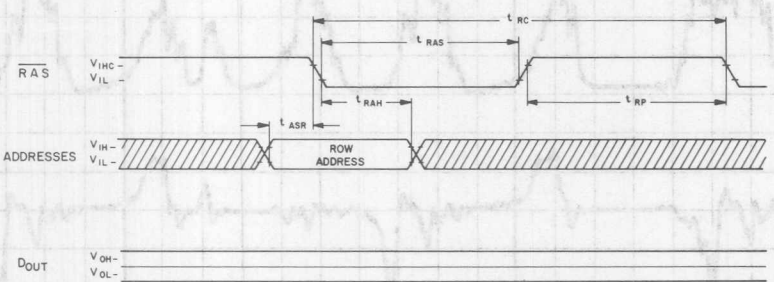
Note also that there is very small DC component in the current waveforms, independent of how long the address strobes remain active. This is because most of the circuitry in the MK 4027 is dynamic, with the exception of the $\overline{RAS}$ input buffer.

The first portion of the current waveforms illustrates a normal $\overline{RAS}$/$\overline{CAS}$ memory cycle. As expected, the I_{DD} waveform has three major current peaks above ground level. These occur when $\overline{RAS}$ goes active, then when $\overline{CAS}$ internally goes active, and finally when both $\overline{RAS}$ and $\overline{CAS}$ go back into precharge. On the other hand, both positive and negative current transients are associated with I_{BB}. This results in peak currents that can be two to four orders of magnitude higher than the average D C value.

The second cycle is representative of a page-mode cycle in which $\overline{CAS}$ is completely enveloped by $\overline{RAS}$.

"RAS ONLY" REFRESH CYCLE

Figure 11



iated with RAS and CAS going into precharge simultaneously. Instead, two smaller current spikes are generated, each coinciding with the separate termination of $\overline{CAS}$ and $\overline{RAS}$. From the current waveform it is clear that approximately 60% of all active power is due to $\overline{RAS}$ and only about 40% of all active power is due to $\overline{CAS}$. Thus, even with increased frequency, the maximum power dissipated in a page-mode operation is less than that in a normal cycle.

The third cycle is a "$\overline{RAS}$-only" cycle which can be used for the refresh operation. Note that the MK 4027 will dissipate considerably less power when the refresh operation is accomplished with a "$\overline{RAS}$-only" cycle as opposed to a normal $\overline{RAS}/\overline{CAS}$ cycle.

TESTING THE MK 4027 MEMORY DEVICE

Production testing of each MK 4027 memory device begins early in the process of every MK 4027 wafer. Once a wafer is processed, each individual die on that wafer is subjected to probe testing. This is where each die is probed and tested for functionality, leakage and continuity. All die that pass this test are then packaged and subjected to further Quality Assurance Processing.

The next barrage of tests include the following:

100% Pre-burn testing at high temperature (for function, leakage, and continuity)

100% Dynamic Burn-In - each device is operated at conditions well beyond data sheet limits for many hours to insure that only quality devices reach the end user.

All MK 4027 devices that pass the previous tests are then final tested for customer use. At final test, all devices are tested at high temperature, to all data sheet AC and DC specifications with wide guardbands. This type of Quality Assurance Processing and Testing insures that not only does every MK 4027 perform well within the established data sheet limits, but also exhibits the quality and reliability standards necessary for today's (and tomorrow's) data processing applications.

Thorough testing of every MK 4027 is performed on what MOSTEK calls "MASTER TESTERS." These machines incorporate a very versatile pattern generator made by Computest and a very sophisticated parametric measurement unit (PMU) and clock section that was conceived and constructed by MOSTEK Test Equipment design engineers. This combination of purchased and custom designed hardware is controlled by a PDP-11 minicomputer. These MASTER TESTERS are used not only in production testing but also in the engineering characterization of the MK 4027. This permits excellent correlation between characterization and production testing on the device. The test equipment is also used as an analysis tool in

RAS / CAS CYCLE - LONG RAS / CAS CYCLE - RAS ONLY CYCLE
Figure 12

MOSTEK's 4K testing area.

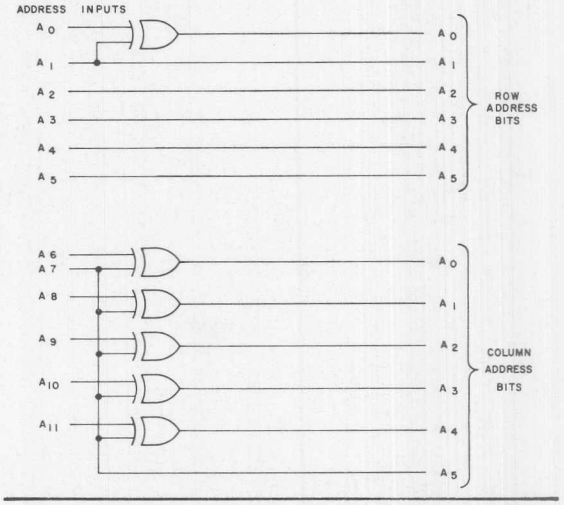
the "continuing engineering" phase of MK 4027 production.

Establishing one's own incoming inspection and testing procedures for a device as complicated as a 4K dynamic RAM is one of the most important and critical procedures in any production program. Usually the effectiveness of the screening procedure may not be known until several assembled systems have been field tested for several months. Therefore, it is important that proper screening procedures are employed early in any production program.

Many times, in establishing electrical end-point tests, it is necessary to know the proper external addressing sequence to insure sequential addressing within a memory device. The internal address bit map of the MK 4027 is arranged in a somewhat unusual fashion to keep the chip size to a minimum. Therefore, sequentially addressing the MK 4027 cannot be done with a straight binary count without the circuitry shown below. Note that this is for testing purposes only and is certainly not required or recommended for system use.

MK 4027 ADDRESS INTERPOLATION

Figure 13



Also, since the sense amplifiers within the MK4027 are located in the center of the memory matrix, data stored in half of the memory will be inverted from the data presented at the input pin. Once again, this inversion is completely transparent to the user (i.e., data stored in the memory as a "1" or "0" at the input will, when subsequently accessed, appear as a "1" or "0" respectively at the output). However, if one wishes to determine the polarity of data stored in the memory, refer to the following chart.

ROW ADDRESS A_5	DATA STORED
0	inverted data
1	true data

III

1982/1983 MEMORY DESIGNERS GUIDE

MOSTEK®

PRINTED CIRCUIT BOARD LAYOUT STRATEGY FOR BYTEWYDE™

Application Note

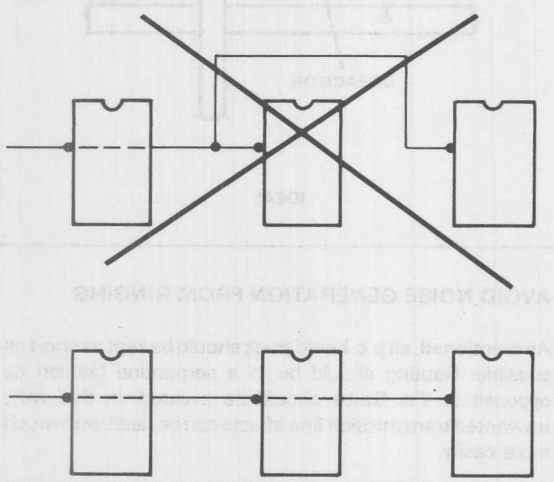
INTRODUCTION

Printed circuit board layout is the process of logically mapping interconnections to the various devices in a system. The number one problem in digital design is noise. Layout techniques have a profound effect on noise. A good strategy is an important part of a good layout. While each p.c. board layout can involve some special considerations, all have similar problems which can be solved with a common set of rules and guidelines. BYTEWYDE™ memory p.c. board layouts have an advantage over other p.c. layouts because of a standardized pinout. Standardization helps promote a simple, symmetrical, and dense layout. The following discussion describes the issues involved with p.c. board layout and how they should be applied to a BYTEWYDE memory design.

USE SYMMETRY

The BYTEWYDE p.c. board should be laid out in a symmetrical pattern. In a symmetrical design all components within the system will be operating under nearly exact conditions because signal paths will be of equal lengths. If problems are encountered, they will relate to all components and are more easily identified. Adherence to the symmetry principle minimizes position sensitivities of a memory matrix allowing for uniform operation. The insidious problems of random and occasional errors are avoided.

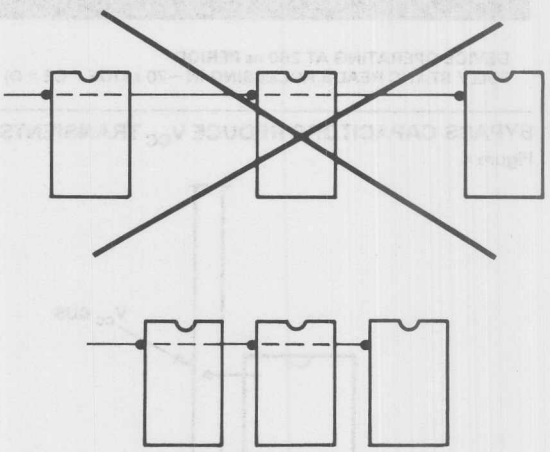
SYMMETRY
Figure 1



STRIVE FOR DENSITY

The memory array should be packed as dense as possible. Closely spaced components help keep all signal paths short. As line lengths are shortened, the unwanted effects of ringing, crosstalk, and propagation delay are minimized. Density also provides the economic advantage of low real estate cost per bit of memory.

DENSE MATRIX KEEPS SIGNAL LINES SHORT
Figure 2



IV

AVOID NOISE GENERATION FROM I_{CC} TRANSIENTS

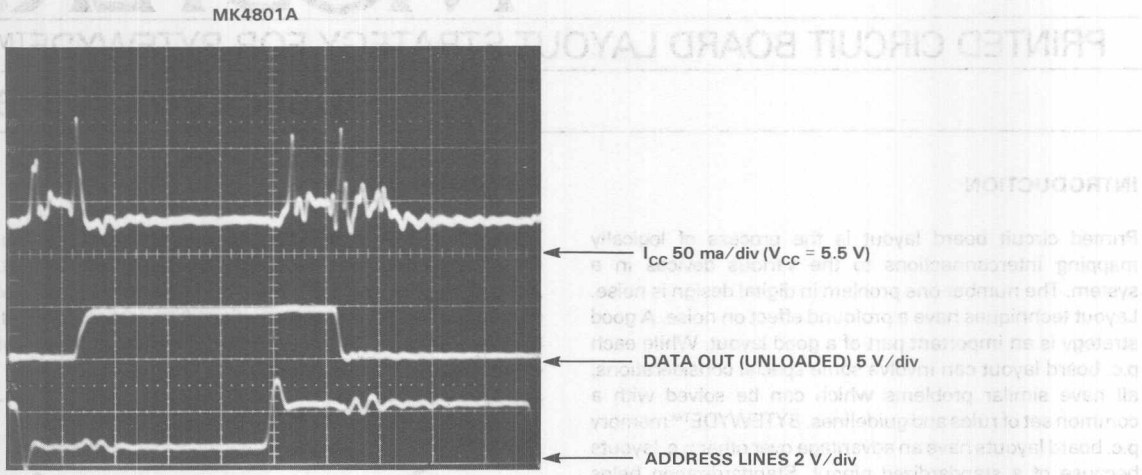
Bypass capacitors are needed in p.c. board memory design to reduce I_{CC} transients. Transients are generated when memory devices go into active cycle and when output buffers turn on and off. The capacitors are used as small energy reservoirs which can supply instantaneous current demands of the memory.

BYPASS CAPACITORS REDUCE V_{CC} TRANSIENTS

I_{CC} transients produce fluctuations which results in spikes on the bus. These can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored by the bypass capacitors will be released as low going spikes are generated and energy will be absorbed as overshoots occur. Due to the fast fall and rise time of the V_{CC} transients, capacitors with good high frequency response, located as close to the memory package pins as possible to reduce inductance, are needed for proper filtering.

CURRENT TRANSIENTS ARE GENERATED AS MEMORY DEVICES GO INTO CYCLE

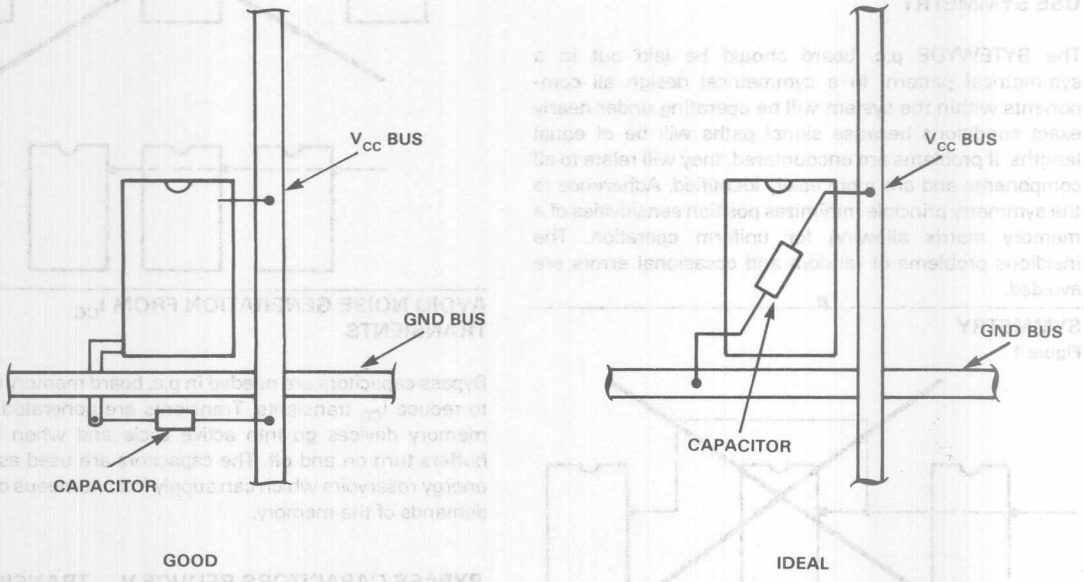
Figure 3



DEVICE OPERATING AT 250 ns PERIOD
FULLY STATIC READS ACCESSING IN ~70 ns (OE = CE = O)

BYPASS CAPACITORS REDUCE V_{CC} TRANSIENTS

Figure 4



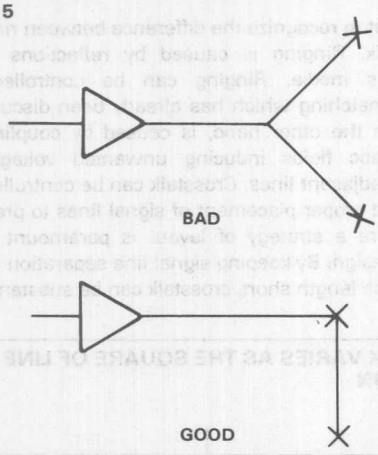
Bypass capacitor value of .1 μf is more than sufficient storage capacity to provide the needed filtering action from the equation $C=I\Delta t/\Delta V$. If I=150 ma and ΔV=1 volt, a capacitor value of .1 μf will filter a 666 ns noise spike. This is well within the cycle time of the memory. The .1 μf capacitor is an economical size and applying a rule of thumb of one capacitor per package gives a cost effective solution to V_{CC} transients.

AVOID NOISE GENERATION FROM RINGING

As mentioned, all p.c. board track should be kept as short as possible. Routing should be in a serpentine fashion as opposed to Y's. Stubs should be avoided. In this way, unwanted transmission line affects can be dealt with much more easily.

AVOID TRANSMISSION LINE STUBS

Figure 5

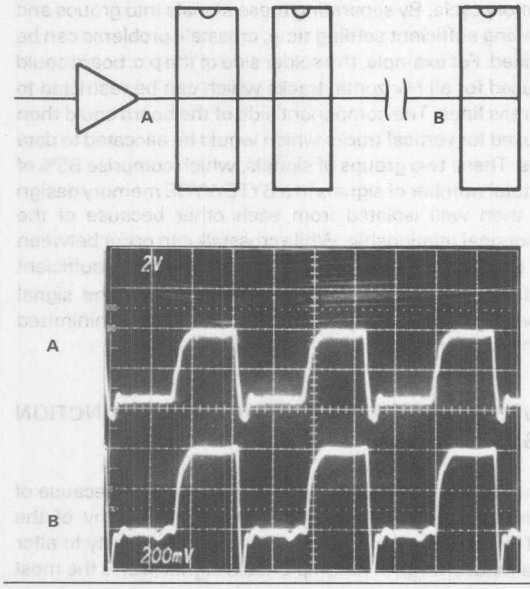


RINGING RESULTS FROM LONG UNTERMINATED LINES

As a rule of thumb, ringing becomes a problem when the propagation delay of a line becomes longer than the rise and fall time of an applied signal (propagation delay of G10 glass epoxy ≈ 2 ns/ft). Although rise and fall times vary with the different logic families, track length shorter than six inches generally causes no ringing problems. In some designs long runs of p.c. track cannot be avoided. Rise and fall times of signals can be increased to compensate for long signal paths, but, in many cases, the reduced performance which results cannot be traded off. When these types of circumstances exist, ringing must be avoided by proper termination of lines.

RINGING RESULTS FROM LONG UNTERMINATED LINES

Figure 6

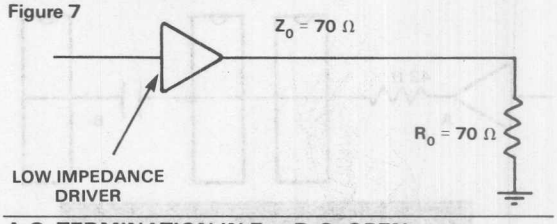


TREAT INTERCONNECTIONS AS TRANSMISSION LINES

Z_0 of a conductor in free space is 377 Ω. This changes rapidly as ground is brought into the proximity of the conductor which lowers Z_0. Two-sided G10 glass epoxy p.c. board track generally has a Z_0 between 70 and 120 ohms depending on the proximity of ground to the signal trace. Impedance matching by proper termination of a transmission line is a way of eliminating ringing. If the load impedance and line impedance are perfectly matched, then no ringing will exist and energy will be dissipated by the load. This ideal condition is difficult to achieve because of the large voltage swings of TTL logic. If Z_0 is assumed to be 70 Ω and the voltage swing is 3.5 volts, then the driver would have to supply 49 ma to drive the load.

TERMINATED TRANSMISSION LINE

Figure 7



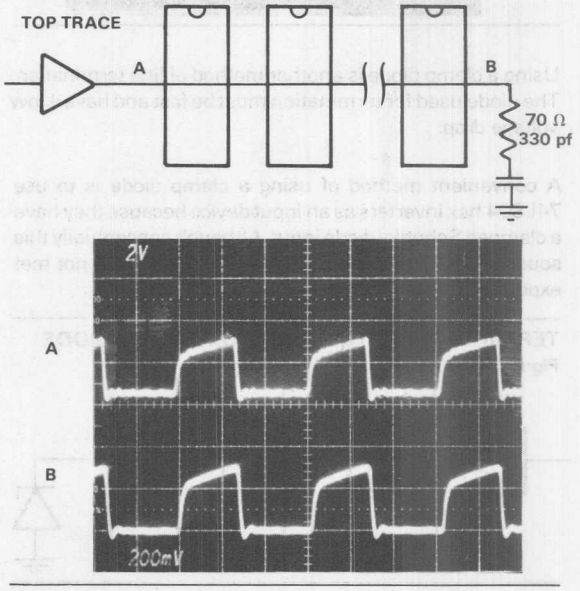
A.C. TERMINATION IN Z_0 - D.C. OPEN

A method of solving the drive problem is to substitute an A.C. termination in Z_0 which will provide a D.C. open circuit.

The A.C. termination has the disadvantage of degrading the rise and fall time of the signal, but at least full logic swing is achieved for D.C. condition which guarantees noise immunity.

AC TERMINATION IN Z_0 ~ DC OPEN

Figure 8



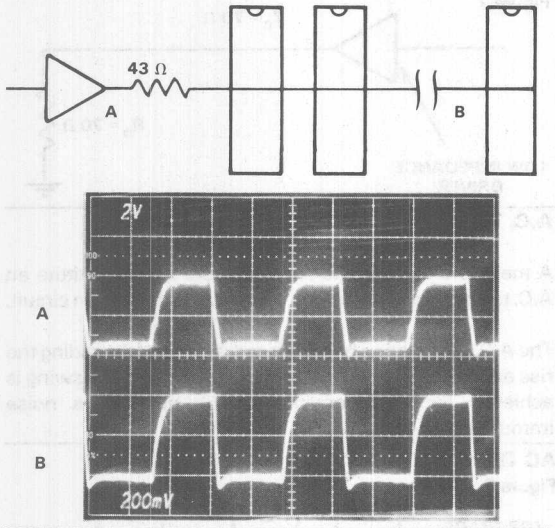
IV

this type of termination, the resistor should be located as close to the driver as possible.

When the signal propagates down the line and sees a reflection coefficient of an open line (+1), it will bounce back down the line towards the series resistor. As the signal arrives back at the series resistor, the reflection will be absorbed after a single bounce. The series resistor will affect the rise and fall time of the signal due to its combination effect with the capacitance of the line (RC). A resistor value of 43 ohms is a good compromise between minimum reflections and poor rise and fall time.

SERIES RESISTOR DAMPS REFLECTIONS

Figure 9

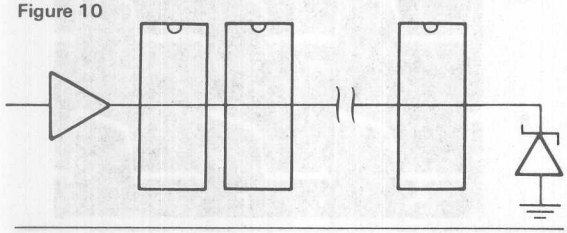


Using a clamp diode is another method of line termination. The diode used for termination must be fast and have a low voltage drop.

A convenient method of using a clamp diode is to use 74LS04 hex inverters as an input device because they have a clamped Schottky diode input. Although conceptually this sounds good, experimental tests at Mostek have not met expectations.

TERMINATING WITH A REVERSE BIASED DIODE

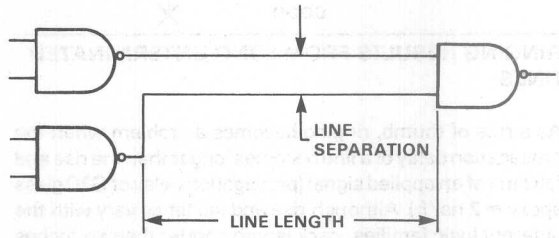
Figure 10



and crosstalk. Ringing is caused by reflections in a discontinuous media. Ringing can be controlled by impedance matching which has already been discussed. Crosstalk, on the other hand, is caused by coupling of electromagnetic fields inducing unwanted voltage or current into adjacent lines. Crosstalk can be controlled by shielding and proper placement of signal lines to prevent coupling. Here a strategy of layout is paramount to a successful design. By keeping signal line separation large and signal line length short, crosstalk can be substantially reduced.

CROSSTALK VARIES AS THE SQUARE OF LINE SEPARATION

Figure 11



ORTHOGONAL RELATIONSHIPS BETWEEN ADDRESS AND DATA LINES

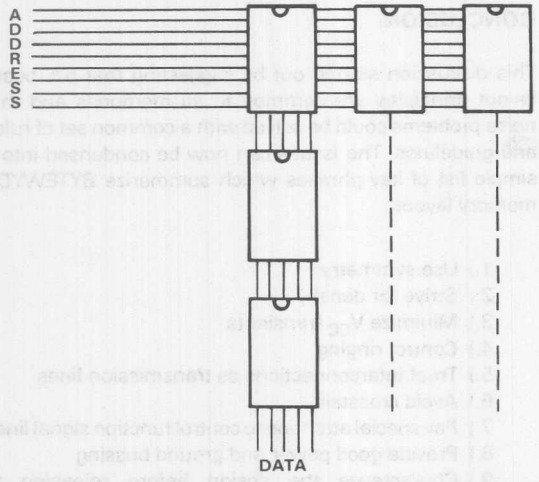
Memory design offers an advantage over random logic because a repetitious pattern can be employed to reduce crosstalk. Well separated, short signal lines can be quite a challenge in a dense BYTEWYDE memory board layout where real estate is at a premium. Address line transitions and data line transitions occur at different times in a memory cycle. By separating these signals into groups and allowing sufficient settling time, crosstalk problems can be avoided. For example, the solder side of the p.c. board could be used for all horizontal tracks which can be restricted to address lines. The component side of the board could then be used for vertical tracks which would be allocated to data lines. These two groups of signals, which comprise 85% of the total number of signals in a BYTEWYDE memory design are then well isolated from each other because of the orthogonal relationship. While crosstalk can occur between the different address lines, it can be ignored if sufficient settling time is allowed in the design before the signal information is used. Crosstalk on the data lines is minimized in the same manner.

GIVE SPECIAL ATTENTION TO CONTROL FUNCTION SIGNAL LINES

Control signals deserve special considerations because of their effect on the power consumption of many of the BYTEWYDE memory components and their ability to alter data inadvertently. The Chip Enable signal ($\overline{CE}$) is the most

ORTHOGONAL RELATIONSHIPS BETWEEN ADDRESS AND DATA LINES

Figure 12

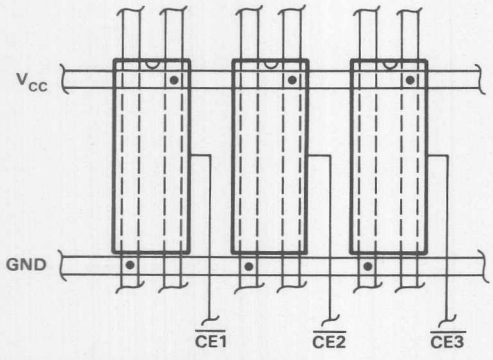


important control function to consider since it powers up the part which is selected to go into cycle. The current transients which occur as $\overline{CE}$ goes active can generate significant noise. $\overline{CE}$ should be isolated from other signal lines by running it adjacent to power and ground lines, thus effectively shielding it from external electromagnetic fields.

Care should also be taken when routing the Write Enable ($\overline{WE}$) and the Output Enable ($\overline{OE}$) control signals. False signals could cause inadvertant data change in the case of $\overline{WE}$ and bus contention in the case of $\overline{OE}$. All three control signals should be isolated from each other and from other signal lines as much as possible.

ISOLATE THE CHIP ENABLE

Figure 13

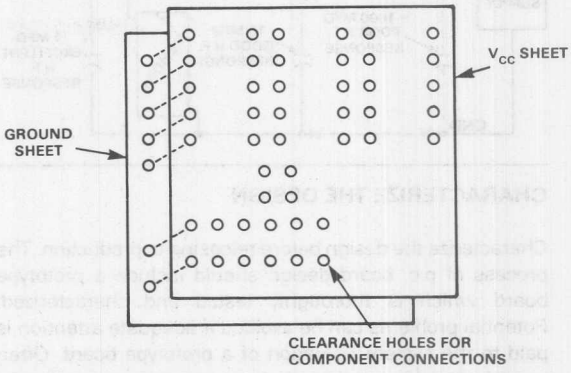


PROVIDE GOOD POWER AND GROUND BUSSING

Good power and ground bussing is essential to prevent noise generation from I_{CC} transients and provide shielding for the various signal lines. Ideally, a separate ground and V_{CC} sheet should cover the entire printed circuit board. This is not possible because there would be no room for signal traces. A multilayered circuit board with a separate layer for V_{CC} and one for ground would be a solution, but this significantly adds to cost. Furthermore, it is complicated because of clearance holes which are provided to make connection to the various components.

MULTI-LAYERED CIRCUIT BOARD PROVIDES OPTIMUM POWER AND GROUND DISTRIBUTION

Figure 14

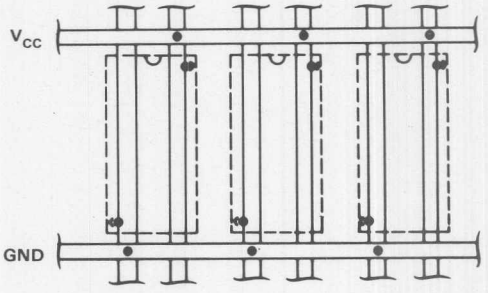


The multi-layered circuit board provides a good solution to power and ground bussing. However, a fully gridded power and ground bussing system provides a satisfactory solution for most designs within the economics of two sided printed circuit boards.

IV

FULLY GRIDDED GROUND AND POWER BUSSING

Figure 15



SYSTEM ENERGY STORAGE

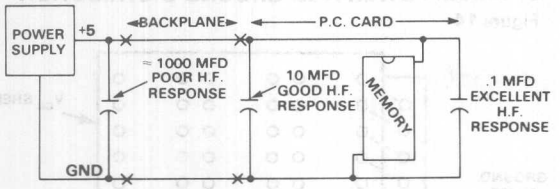
The power and ground system should have sufficient capacitance to absorb current transients. This issue was addressed earlier in this text with some discussion about bypass capacitors. These capacitors provide filtering for the transients generated by the individual components. However, overall system power distribution needs to be given attention.

Substantial transients are also caused by multiple devices switching in unison, such as address lines or data lines over the back plane. Here a capacitor at the edge connector can smooth this type of current fluctuations. The type of capacitor needed at the p.c. board edge must be larger in size and can be less critical in terms of frequency response

than the bypass capacitors. The need for larger capacitors to compensate for distributed inductance continues all the way to the system power supply.

SYSTEM ENERGY STORAGE

Figure 16



CHARACTERIZE THE DESIGN

Characterize the design before releasing to production. The process of p.c. board design should include a prototype board which is thoroughly tested and characterized. Potential problems can be avoided if adequate attention is paid to the system operation of a prototype board. Often small improvements to the layout can reduce noise. A good technique is to individual probe each signal line of the memory for waverform integrity, and compliance to data sheet specifications. Operating margin can be assured by varing the temperature and supply voltage of over expected range. The proper time to locate and correct problem areas is prior to committing the design to production where the mistakes multiply rapidly.

CONCLUSION

This discussion started out by suggesting that p.c. board layout principles are common to all memories and that noise problems could be solved with a common set of rules and guidelines. The issues can now be condensed into a simple list of key phrases which summarize BYTEWYDE memory layout.

1.) Use symmetry
2.) Strive for density
3.) Minimize V_{CC} transients
4.) Control ringing
5.) Treat interconnections as transmission lines
6.) Avoid crosstalk
7.) Pay special attention to control function signal lines
8.) Provide good power and ground bussing
9.) Characterize the design before releasing to production

By employing good design practices and by executing this check list of key phrases for BYTEWYDE memory design, problems can be avoided.

MOSTEK®

NMOS RAM OFFERS NON-VOLATILITY WITH DATASAVE™

Application Note

INTRODUCTION

Non-volatile memory presents a paradox. On the one hand, data must be conveniently changed, while on the other hand, data must be safeguarded against loss. This problem can be likened to a door with a simple lock for normal entry, and a dead bolt latch for security. The non-volatile memory must have a simple method of purposeful change of data, yet have absolute protection against inadvertent loss of data.

At the system level storage requirements vary and not all memory need be non-volatile. In the past, memory was partitioned with regards to what must be retained and what could be lost. ROM and PROM were used for non-volatile storage, and RAM for volatile or temporary storage. The BYTEWYDE™ concept of RAM, ROM, and EPROM interchange has added flexibility to this type of memory design. The flexibility of memory interchange relieves many of the problems associated with predicting how much and what type of memory is needed. But there are many applications where interchange of memory is not enough. These designs are typified by the need to alter non-volatile memory.

Non-volatility is related to how difficult a device is to program or restrictions on the write cycle. ROM, for example, is factory programmable and is totally non-volatile. UV EPROMs can be altered in the field with some time and difficulty. UV EPROMs, and similar devices, have reduced non-volatility to a degree of inconvenience. The difficulty of altering the content of non-volatile memory has led to the development of new storage mechanisms for data retention. Many of the new storge mechanisms for memory are aimed at making the program cycle more closely emulate the read cycle. Ideally, a non-volatile memory should possess the following features:

1) Ease of use.
2) High density.
3) Write cycle performance equal to the read cycle.
4) Infinite number of program or write cycles.
5) High performance.
6) Low power and cost.

Many of the devices on the market have made progress towards meeting the list of requirements for a non-volatile memory. However, each technology explored to date falls somewhat short of what is required. For example, UV EPROMs need UV light for erasure and have a long program cycle. E^2PROMs, while being more convenient with electrical erasure, still have a long erase/program cycle and a limited number of write cycles. Shadow RAMs solve the write or program cycle problem, but have low densities because of the more complex cell.

A battery backup RAM can be a viable alternative to new technology methods of non-volatility if certain conditions exist. In order to be an effective solution, a battery backup RAM must use low power and be easy to implement. CMOS RAMs meet the low power requirement, however, the increase in processing needed for CMOS leads to higher cost. In fact, the most dense CMOS RAM available uses the same cell that has been used in Mostek static NMOS memory since 1977.

IV

Proven NMOS memory technology combined with an innovative circuit design called DATASAVE is being introduced by Mostek. This 2K x 8 BYTEWYDE RAM, coupled with the advancements made in battery technology, bridges the gap between non-volatile memory and existing static RAM design (see Figure 1). The MK48D02 (DATASAVE) provides data retention using on chip circuits which switch to a standby battery when primary power failure occurs. A standby current of only 100μA is needed, since only the memory matrix and minimal support circuitry are maintained during the data retention mode. Low battery drain, ease of use, unlimited write cycles, read cycle equal to write cycle, and high performance make the MK48D02 an attractive offering.

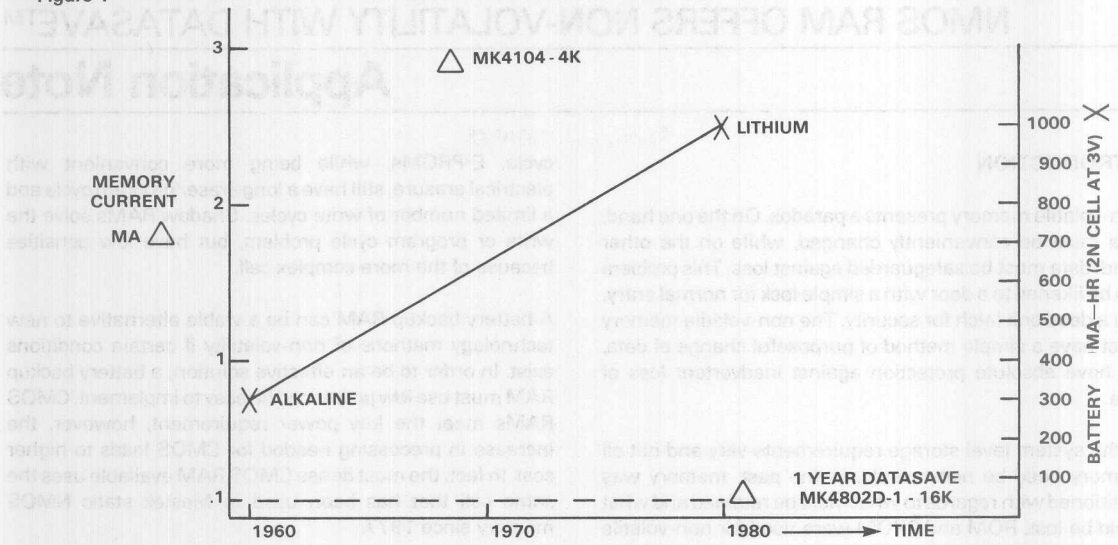
HOW IT WORKS

To accomplish the data retention mode, several new circuits and low power memory cells have been incorporated into the MK48D02. The new circuits consist of a voltage comparator which senses the status of V_{CC}, a switch to allow current to be sourced to the internal memory matrix from the $\overline{WE}$ pin instead of V_{CC}, and a standby charge pump needed to compensate for voltage changes, which are capacitively coupled to the substrate, when switching from DATASAVE.

The key to DATASAVE is the comparator and switch which put the memory in an ultra-low power write protected state (see Figure 2). The comparator monitors the status of V_{CC} and $\overline{WE}$. When $\overline{WE}$ is greater than V_{CC} by one volt ($\overline{WE} > V_{CC}$-1), the comparator output will activate a transistor switch connecting the $\overline{WE}$ pin to the memory matrix and inhibit all inputs/outputs. The memory matrix current will

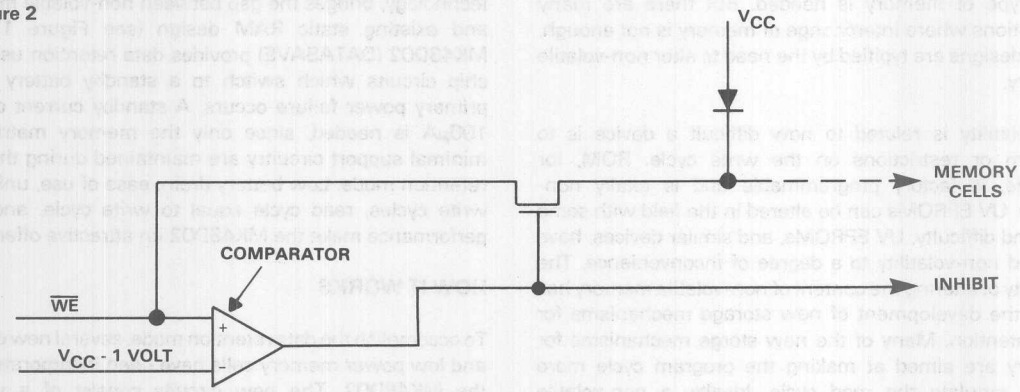
NON-VOLATILITY

Figure 1



MOSTEK'S DATASAVE™ ON CHIP FEATURE

Figure 2



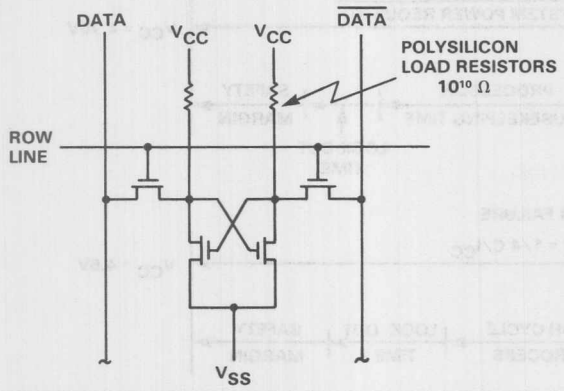
be sourced through the $\overline{WE}$ pin. All other circuits, with the exception of a standby charge pump and inhibit logic for the I/O, will become inactive as V_{CC} falls below write enable ($\overline{WE}$).

The standby charge pump provides bias which prevents the substrate from going positive during power up. This charge pump is a low power version of the larger charge pump which is active when V_{CC} is within specification.

The MK48D02 uses a low power cell consisting of intrinsic polysilicon resistors (see Figure 3) instead of the more power consuming depletion mode transistors. The low power is achieved because the resistor value is of the order of 10^{10} ohms. Total matrix pull up current for thirty-two thousand resistors is approximately 30 μA. The resistors also help reduce cell size by permitting an efficient layout. Using Mostek's POLY 5 process, cell size is a mere 1.3^2mils.

LOW POWER CELL

Figure 3



SPECIFIC REQUIREMENTS

In order to successfully use DATASAVE, it is necessary to switch the $\overline{WE}$ pin from its normal function to the battery voltage prior to power failure. Battery supply to the $\overline{WE}$ pin during DATASAVE must be held between 4.0 volts and 6.0 volts. External supply current to the memory is approximately 50μA during DATASAVE. Power supply slew rates need to be limited to 200μs/volt (see Figure 4).

Power supply slew rate is a function of power supply design. The selection of the power supply used for V_{CC} in any battery backup design is an important matter. The power supply must have sufficient energy storage to hold V_{CC} within specification for some time after A.C. power is lost and meet the voltage slew rate specifications of the MK48D02 (see Figure 5). The proper selection of a power supply still does not solve the energy storage problem completely. Certain conditions, such as power supply malfunctions, blown fuses, etc., make it a wise precaution to have some additional storage capacity distributed throughout the system. Bypass capacitors provide some energy storage. However, the energy stored is far less than what is required. This can be illustrated by the following example. Assume a bypass capacitor size of .1MFD. Then C = I $\Delta t/\Delta V$ with ΔV = 1 volt and I = 125 MA (from the MK48D02 specifications) gives a slew time of .8μs. This exceeds the ΔV specified for the MK48D02. Energy storage must be supplemented with additional capacitance located at various points along the V_{CC} bus.

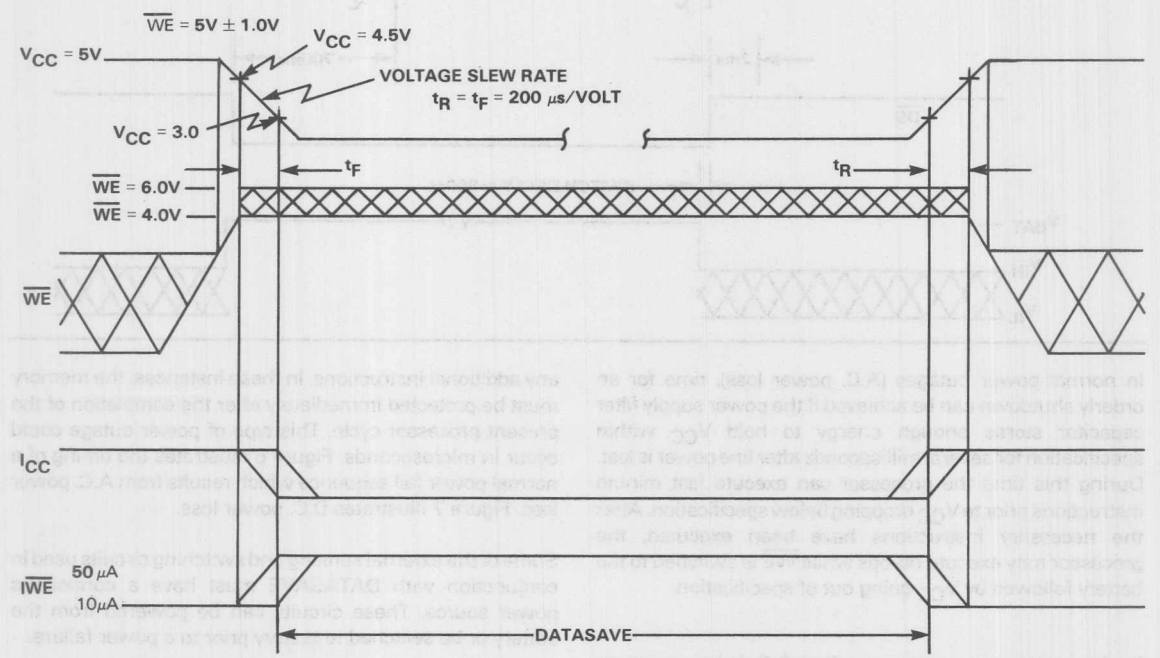
BATTERY BACKUP DESIGN

A sound battery backup design must be able to handle all types of power interruptions. Two power failure signals are required. One signal continuously defines the state of V_{CC}, while a second defines a change in the status of the power line.

IV

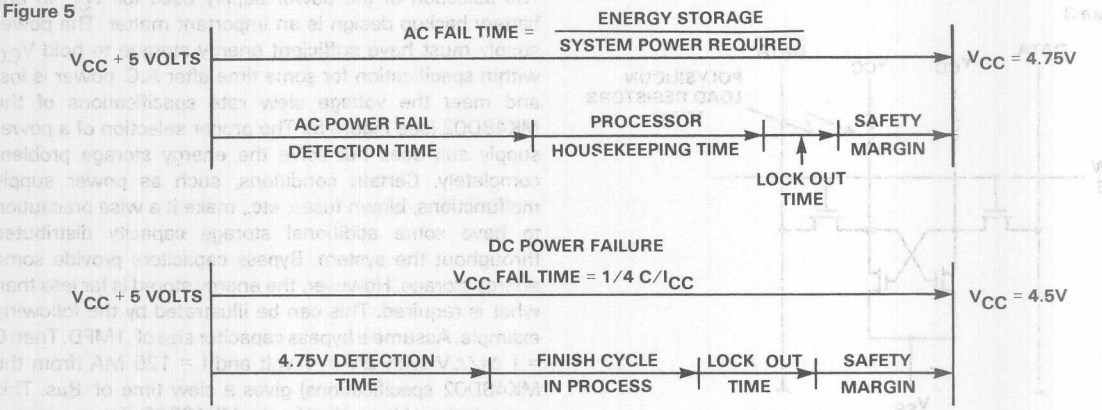
DATASAVE POWER SUPPLY REQUIREMENTS

Figure 4



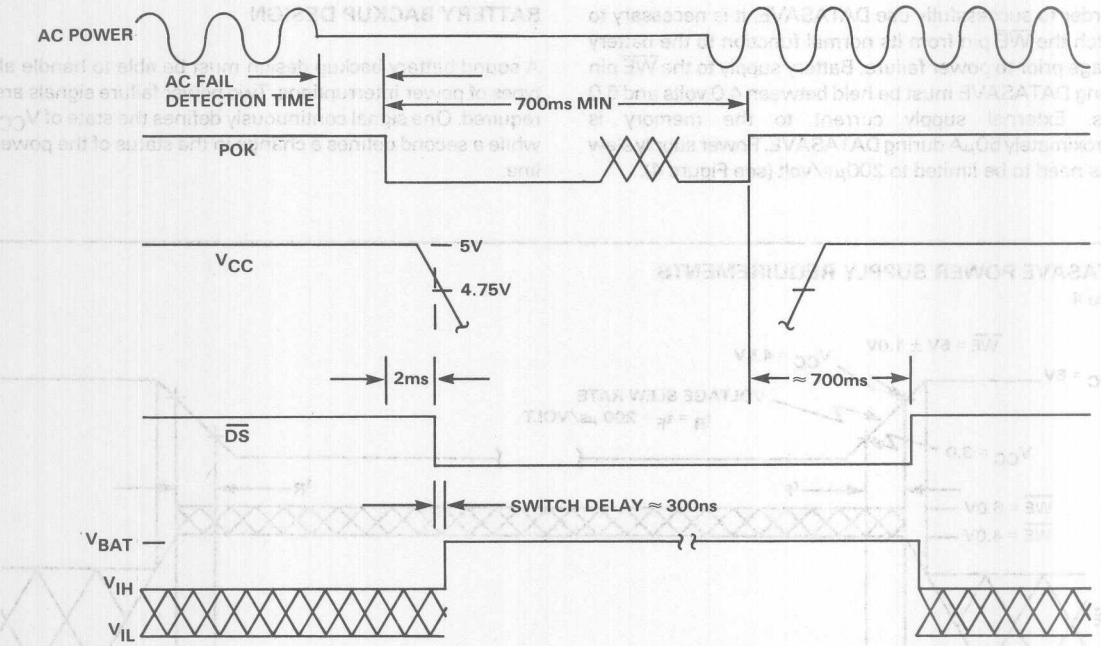
AC POWER FAILURES

Figure 5



AC POWER FAILURE SEQUENCE

Figure 6



In normal power outages (A.C. power loss), time for an orderly shutdown can be achieved if the power supply filter capacitor stores enough energy to hold V_{CC} within specification for several milliseconds after line power is lost. During this time the processor can execute last minute instructions prior to V_{CC} dropping below specification. After the necessary instructions have been executed, the processor may execute no-ops while $\overline{WE}$ is switched to the battery followed by V_{CC} going out of specification.

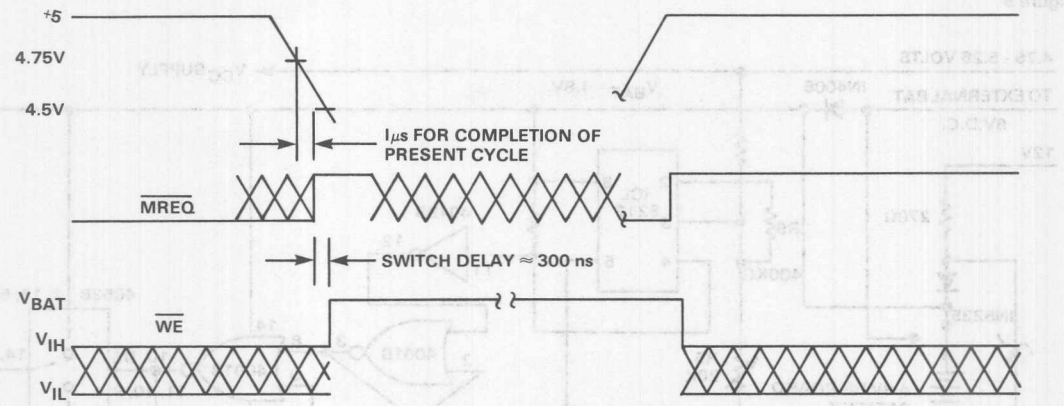
In abnormal power outages, such as D.C. failure or power brown outs, there may not be time for the processor to do any additional instructions. In these instances, the memory must be protected immediately after the completion of the present processor cycle. This type of power outage could occur in microseconds. Figure 6 illustrates the timing of a normal power fail sequence which results from A.C. power loss. Figure 7 illustrates D.C. power loss.

Some of the external sensing and switching circuits used in conjunction with DATASAVE must have a continuous power source. These circuits can be powered from the battery or be switched to battery prior to a power failure.

Battery choice is a function of application and selection

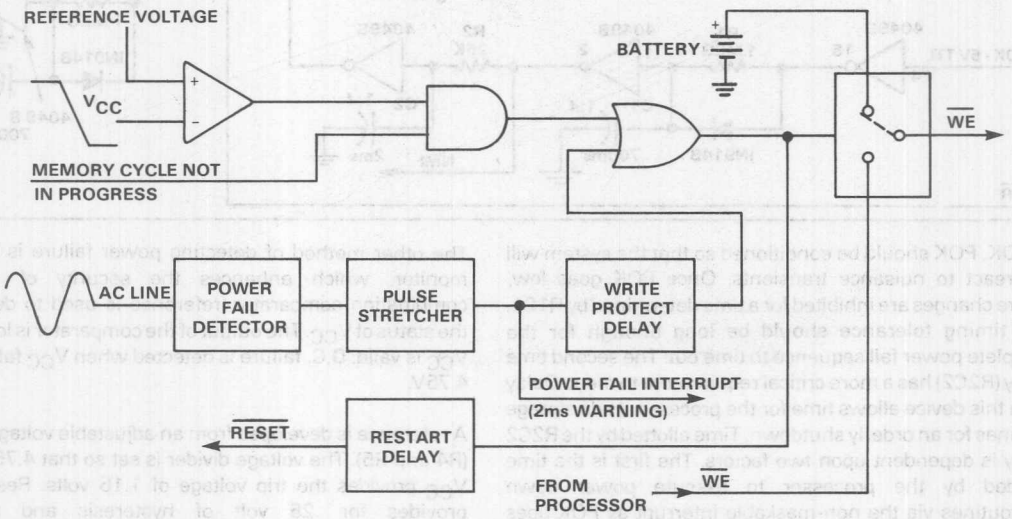
DC POWER FAILURE SEQUENCE

Figure 7



SYSTEM BLOCK DIAGRAM

Figure 8



should be based on performance and economy needed. A rechargeable battery should be used where power is constantly drained from the battery.

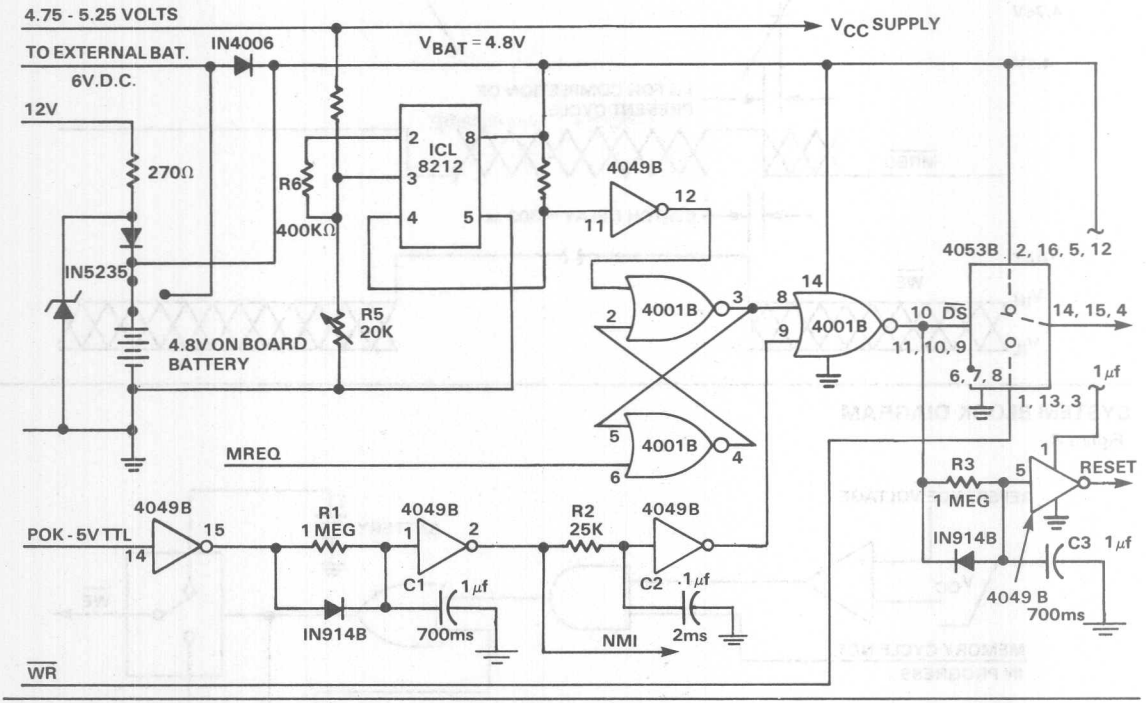
AN ACTUAL DESIGN

A circuit was designed to illustrate the usefulness of the DATASAVE feature in a system. The design requirements to be met in this application are as follows:

1) Sufficient battery to support 16K x 8 memory for 72 hours.
2) Foolproof power fail detection system.
3) Low battery drain current from the memory support circuitry.
4) Timing circuitry to allow for a microprocessor to do an orderly shutdown and automatic restart.
5) In-circuit battery charging.
6) Optional disposable batteries for economical designs.

In order to meet the above criteria, the logic of the system was designed to handle the two types of power interruptions (see Figure 8 for system block diagram). The normal shutdown is accomplished by sensing A.C. power line conditions. An A.C. line monitor must be used to convert the power line status to TTL levels. The A.C. power fail detector gives a low going TTL transition prior to V_{CC} going out of specification. This TTL signal, called Power OK or POK (see Figure 9), then creates a series of timed events. The first timing device provides a delay on the trailing edge

Figure 9



of POK. POK should be conditioned so that the system will not react to nuisance transients. Once POK goes low, future changes are inhibited for a time determined by R1C1. The timing tolerance should be long enough for the complete power fail sequence to time out. The second time delay (R2C2) has a more critical requirement to meet. Delay from this device allows time for the processor to do storage routines for an orderly shutdown. Time allotted by the R2C2 delay is dependent upon two factors. The first is the time needed by the processor to execute power down subroutines via the non-maskable interrupt as POK goes low. The second factor is the time the power supply can hold V_{CC} within specification after A.C. failure has occurred. The two restrictions on time need to be tailored to exact system needs. The 2MS of time, which is allotted in this design, is more than sufficient for the processor to do housekeeping. More time can be made available if the power supply used can hold V_{CC} in specification longer. In applications where the amount of time required is critical, more accurate timing elements and more energy storage can be used.

The output of the second time delay is one of two signals which can activate DATASAVE. A third time delay, R3C3, is required for automatic startup of the processor. R3C3 time needs to be long enough for V_{CC} to stabilize prior to turning control back to the processor since it restarts processor controlled memory cycles. For this design, an R3C3 time of 700MS was used.

The other method of detecting power failure is the D.C. monitor, which enhances the security of data. A combination comparator/reference is used to determine the status of V_{CC}. The output of the comparator is low when V_{CC} is valid. D.C. failure is detected when V_{CC} falls below 4.75V.

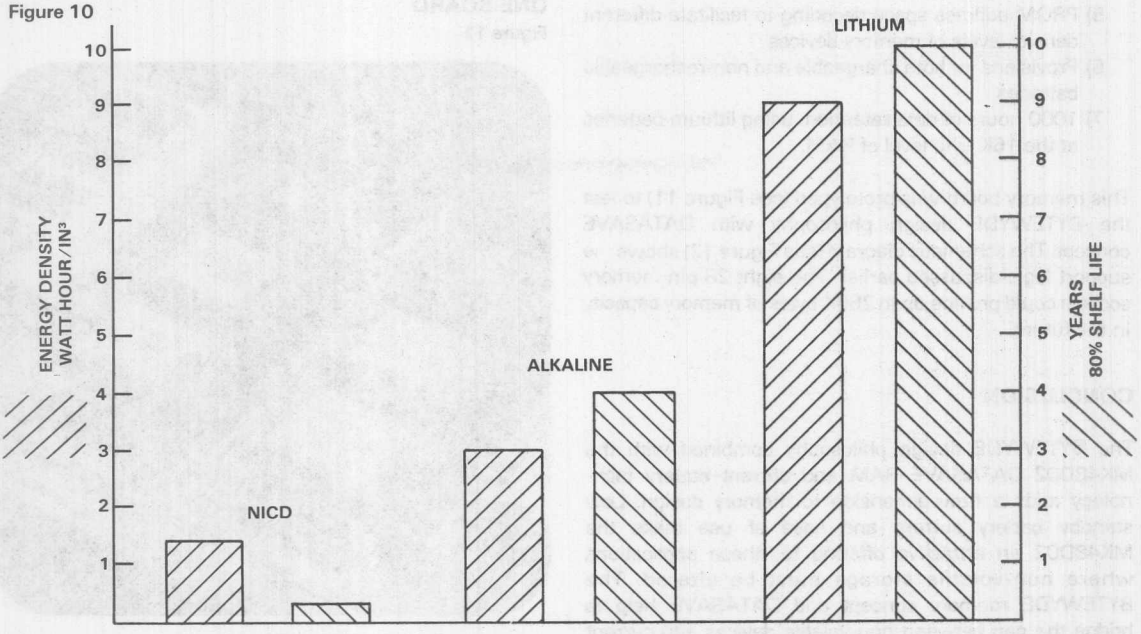
A reference is developed from an adjustable voltage divider (R4 and R5). The voltage divider is set so that 4.75 volts at V_{CC} provides the trip voltage of 1.15 volts. Resistor R6 provides for .25 volt of hysteresis and prevents undetermined outputs from the reference/comparator. The power fail condition readies a NOR flip-flop, which is activated by $\overline{MREQ}$ when the microprocessor goes to a memory inactive high state. When $\overline{MREQ}$ is high, the processor is not doing a memory cycle. The precaution of using $\overline{MREQ}$ to gate D.C. power fail prevents the $\overline{WE}$ line from being interrupted during a write cycle. Failure to take this precaution would mean that information could be lost.

D.C. power fail and POK are or'ed to produce the ($\overline{D.S.}$) DATASAVE signal which controls a CMOS switch. The CMOS switch will disconnect the $\overline{WE}$ pin from processor control and connect the battery supply in typically 300ns. The IR drop across the switch is .08 volt typical for a total memory standby current of 400μA.

The battery supply to support the DATASAVE circuit is

COMPARISON OF DIFFERENT N CELL BATTERY TECHNOLOGY

Figure 10



Technology	NI-CD	Alkaline MnO_2/ZN	Lithium MnO_2/LI
Application	Rechargeable	Non Rechargeable	Non Rechargeable
Cell Voltage	1.2 Volts	1.5 Volts	3 Volts
Size	2 x N Cell	2 x N Cell	2N Cell
MA - HRS	150	300	1000

flexible. If a chargeable battery supply is desired, a jumper-selectable charging circuit can be employed. Non-rechargeable batteries can also be used, and the charging circuit will supply power to the CMOS gates and V_{CC} detector while power is within specification. A blocking diode isolates the non-rechargeable battery during power up conditions. As D.C. power drops below the battery supply, current will start to flow from the battery. This type of arrangement prevents any battery discharge during normal power conditions, so that maximum battery utility is realized.

Battery technology affords a variety of options which can be put to use. High energy density is important for on board batteries. If a non-rechargeable battery is used, lithium batteries afford an inexpensive high energy density solution. Nickel cadmium is a good selection if a rechargeable cell is used. More complete protection can be obtained by a combination of rechargeable and non-rechargeable batteries. In such an arrangement, Ni Cd batteries could provide for short term power failures and long shelf life lithium batteries can provide an emergency reserve. Such an arrangement gives added security and protection through redundancy.

The selection of batteries is influenced by several factors. Shelf life, power density, mounting, rechargeability, and cost are important criteria.

Consistent packaging among various battery technologies helps in the selection process by giving the user an option if the requirements of the design changes. Several companies are presently involved in the manufacture of "N" size cell, which are available in Ni Cd, lithium, and alkaline (see Figure 10).

THE MK48D02 AT THE SYSTEM LEVEL

The advantage of a consistent packaging strategy for memories has been well-documented. Mostek's BYTEWYDE concept now takes on a new dimension with the MK48D02. This BYTEWYDE RAM with battery backup is interchangeable with all BYTEWYDE products. To illustrate this point, a complete memory board was designed with the following features:

1) Non-volatile memory using DATASAVE with all support circuitry included.
2) RAM, ROM, EPROM interchange.

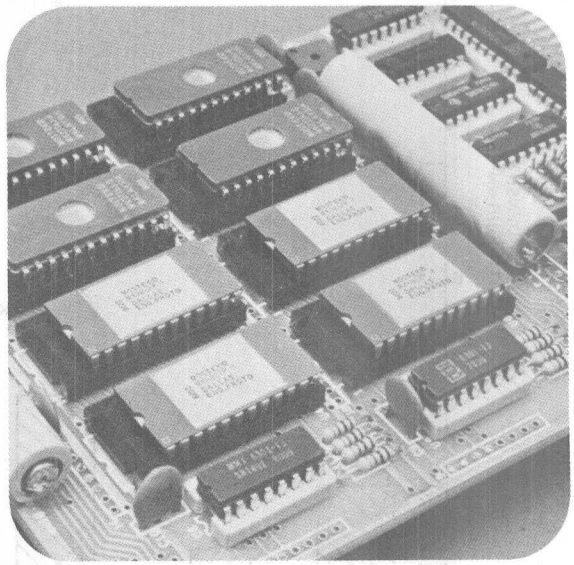
3) STD bus interface.
4) Expandable with technology advancements to 256K bytes of memory.
5) PROM address space decoding to facilitate different density levels of memory devices.
6) Provisions for both chargeable and non-rechargeable batteries.
7) 1000 hours of data retention, using lithium batteries at the 16K byte level of RAM.

This memory board was prototyped (see Figure 11) to test the BYTEWYDE design philosophy with DATASAVE concept. The schematic diagram (see Figure 12) shows ıe support logic discussed earlier. The eight 28 pin memory sockets could provide up to 256K bytes of memory capacity in the future.

CONCLUSION

The BYTEWYDE design philosophy combined with the MK48D02 DATASAVE RAM and current battery technology adds a new dimension to memory design. Low standby battery current and ease of use make the MK48D02 an attractive offering for those applications where non-volatile storage must be altered. The BYTEWYDE memory concept and DATASAVE help to bridge the gap between non-volatile devices and current RAM memories, while providing a better solution to a paradox.

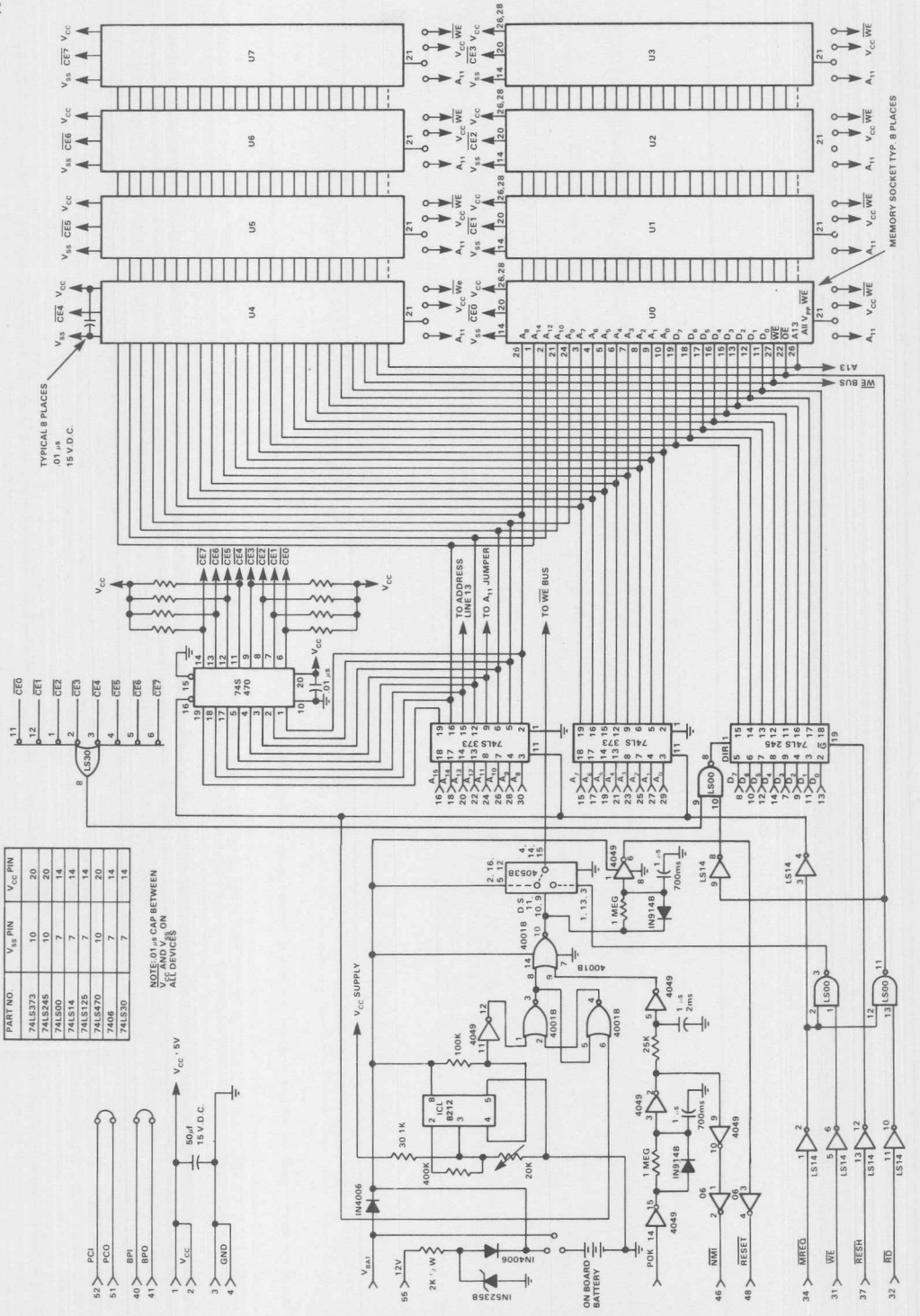
BYTEWYDE MEMORIES WITH DATASAVE CIRCUITS AND STD BUS INTERFACE ON ONE BOARD
Figure 11



Acknowledgements:
W. J. Swain - Designer MK4802D-1
D. K. Lunecki - Product Engineer MK4802D-1

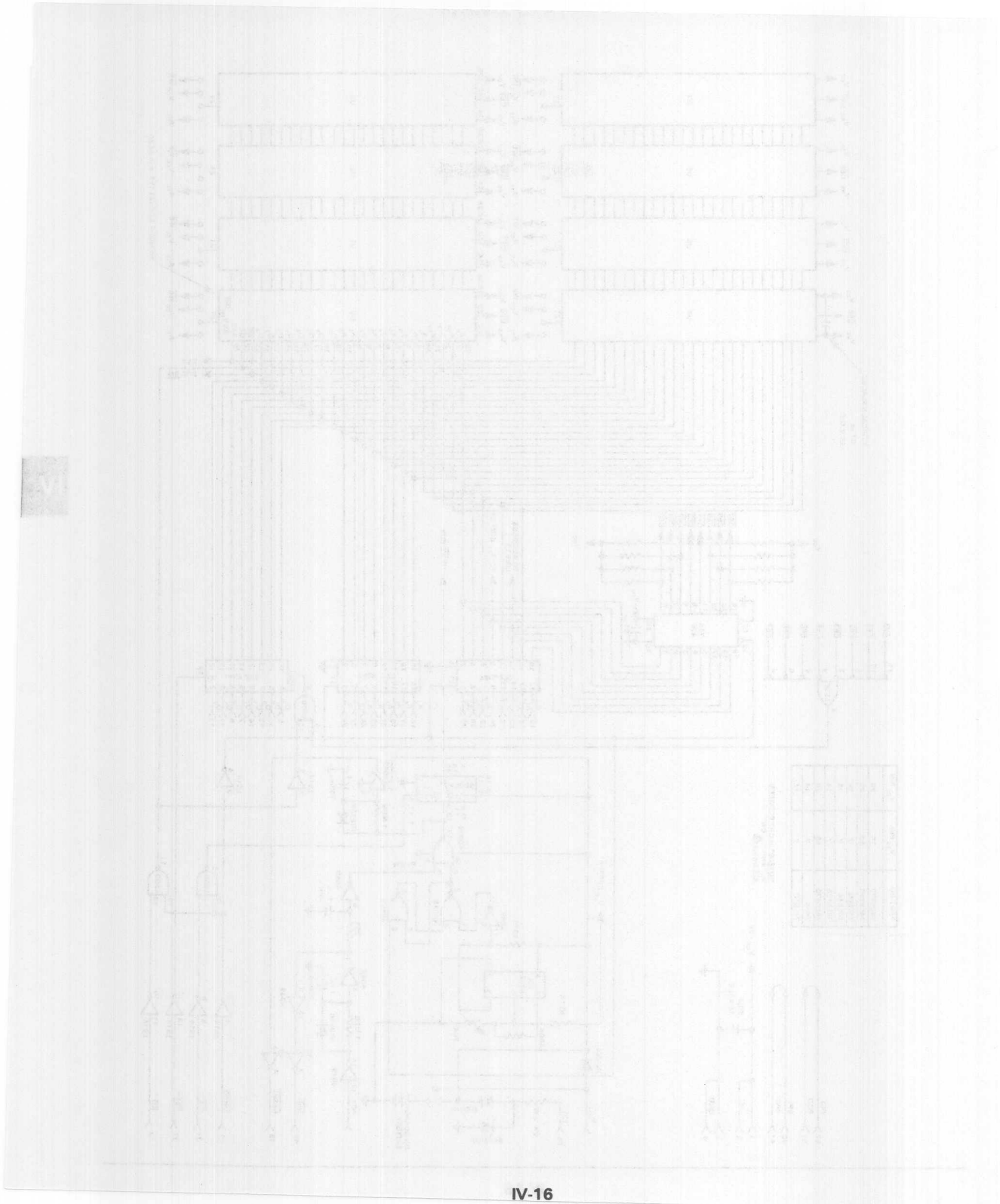
SCHEMATIC DIAGRAM OF THE BYTEWYDE MEMORY BOARD WITH DATASAVE AND STD BUS INTERFACE

Figure 12



PART NO.	V_{SS} PIN	V_{CC} PIN
74LS373	10	20
74LS245	10	20
74LS00	7	14
74LS14	7	14
74LS125	7	14
74LS470	10	20
7406	7	14
74LS30	7	14

IV



MOSTEK®

MK4801A/MK4802 FOR HIGH SPEED APPLICATIONS

Application Note

Designers of high speed memory systems have a new option when it comes to selecting the configuration of their memory array. As N-channel MOS technology follows its customarily aggressive development patterns, two new parts, the 1K x 8 MK4801A and the 2K x 8 MK4802 are becoming available offering density, configuration advantages, and ease of use features not available on 4K density devices. These parts are pin compatible static RAMs utilizing Mostek's POLY 5™ scaled NMOS process. This process combines the density improvement which keeps the die size small for aggressive pricing with the short channel lengths required to place a part in the high speed race.

The relationship between the parts extends beyond similar pinouts and part numbers. The pictures in Figure 1 show the die for both parts and reflect the fact that the MK4802 has a heritage which traces directly to the MK4801A. So the peripheral circuitry and the cell used in both parts are basically the same, with the MK4801A having more maturity while the MK4802 has some design advantages aimed at making the part more versatile.

WHY BYTEWYDE?

Organizing memory chips so that a single IC can interface to a bidirectional data bus is not a new idea; it goes back to small PROMs and to the 6810 256 x 8 static RAM. However, the high density RAM market had effectively ignored the 24 pin by 8 pinout made so popular by EPROMs until the MK4118 was introduced in 1978. This microprocessor-oriented 1K x 8 static RAM is being joined in the market place not only by Mostek's two new static RAMs, but also by a host of other manufacturer's 2K x 8 static RAMs. This flurry of activity validates that the BYTEWYDE™ approach has advantages in certain segments of the market.

The BYTEWYDE concept of memory compatability has taken this base 24 pin package and developed it into a socket compatible family of RAM, ROM, and EPROM. JEDEC has accepted the 28 pin level of density and has used it for the basis of a new memory standard for by 8 parts. Up to now, BYTEWYDE parts like the MK4118 1K x 8 static RAM have served as building blocks with moderate performance aimed at the microprocessor designs. However, many of these benefits carry over to the sub-100ns market.

Fast RAM applications are often in wide word configurations. Video buffers, cache memories, and writable control stores have typical arrangements of 2K x 8, 4K x 32 and 4K x 64, respectively. The benefits of BYTEWYDE which apply to the users are the layout advantage, incremental expansion, density, upward compatability, and the presense of an extra control function.

"FORM FACTORS" OF BY 8 MEMORIES

Advantages of the pinout used in the MK4801A/MK4802 start with the simple fact that these parts are both specification and pin compatible. Once the socket is laid out, the parts are completely interchangeable. This upward compatability is built into the BYTEWYDE pinout. The 28 pin package has sufficient capacity to handle 15 address lines and can accomodate 32K bytes of memory, once the technology can put that on a piece of silicon. Figure 2 shows how the MK4801A/MK4802 fit into this family of parts.

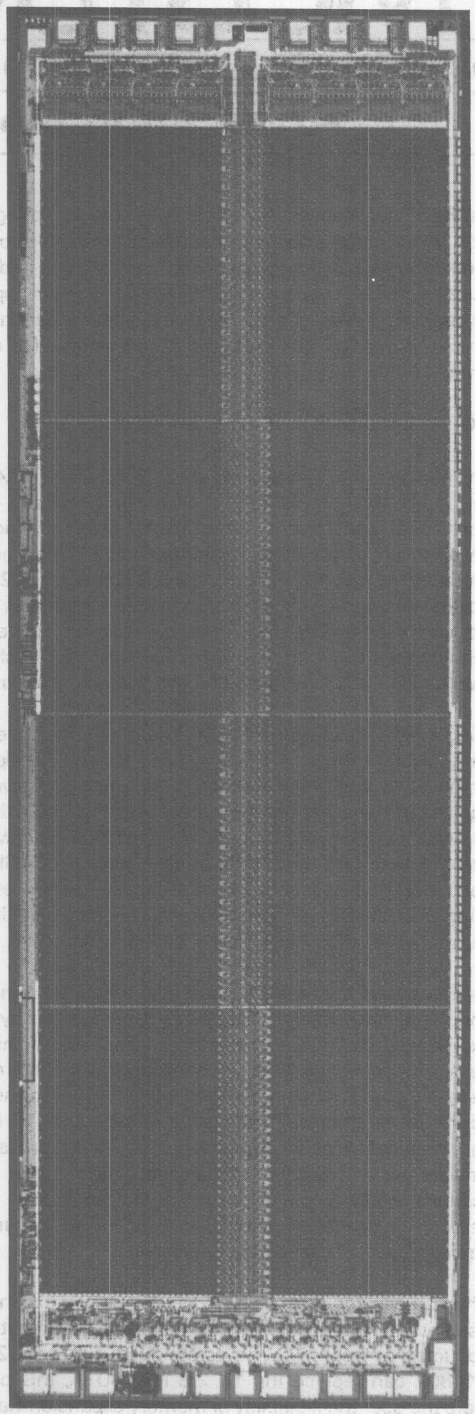
Using a by 8 internal structure has definite advantages for many users from a printed circuit density standpoint, compared to by 1 static memories for applications which require a minimal memory depth relative to word width. For instance, a system requirement needing 8K x 8 of RAM will not be able to take advantage of new generation 16K x 1 products without wasting half of the capacity (the upper 8K). Using BYTEWYDE memories results in better matching of the memory to the actual system configuration.

A side issue of the above argument is that of incremental modular expansion. If a user has by 1 parts in his system and exceeds the capacity of the memory allocated to him by the hardware designer, memory expansion will not come cheap. To go in any additional depth, 8 chips must be added, tacking on another 4K bytes when maybe only 1K bytes were required. Also, since memory expansion represents a considerable hardware modification, the extra chip locations are layed out in anticipation of adding the extra memory chips later. Then if there is no expansion requirement, P.C. real estate was wasted.

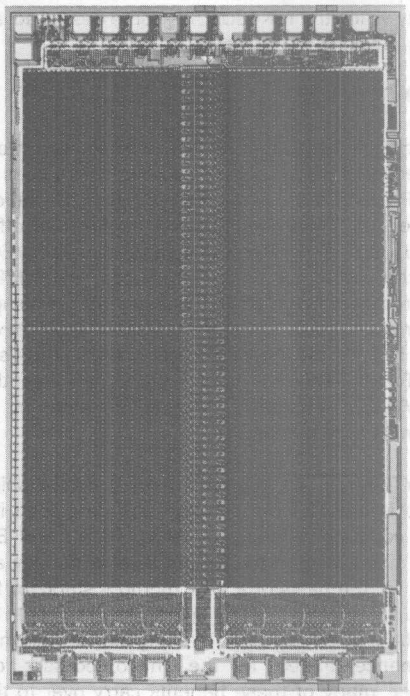
When a designer chooses BYTEWYDE, he can expand the system in 1K byte increments, avoiding manufacturing products that waste P.C. real estate. Also, just as the 2K x 8 MK4802 can replace the 1K x 8 MK4801A, this pinout offers the user the flexability of memory expansion via new higher density 28 pin memory product introduction.

DIE PHOTOGRAPHS

Figure 1



MK4802
Dimensions - 331 mil. x 108 mil.
Area - 35748 sq. mil.



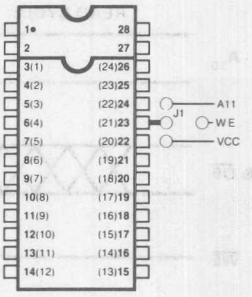
MK4801A
Dimensions - 106mil. x 182 mil.
Area - 19292 sq. mil.

BYTEWYDE TABLE

Figure 2

Memory Type	Part Number	Capacity	Package	Jumper J1
ROM	MK34000	2K × 8	24 Pin	NC
ROM	MK37000	8K · 8	28 Pin	A11
ROM		32K · 8 △	28 Pin	A11
RAM	MK4802	2K · 8	24 Pin	WE
RAM		4K · 8 △	28 Pin	A11
RAM	MK4118A 4801A	1K · 8	24 Pin	WE
EPROM	MK2716	2K · 8	24 Pin	VCC
EPROM	MK2764 △	8K · 8	28 Pin	A11

△ available 1981



4118/A 4801A	4802	34000	2716	4K × 8	37000	32K × 8	2764		2764	32K × 8	37000	4K × 8	2716	34000	4802	4118A 4801A
				NC	NC	A14	NC	1 28	VCC	VCC	VCC	VCC				
				NC	A12	A12	A12	2 27	NC	NC	NC	WE				
A7	A7	A7	A7	A7	A7	A7	A7	3(1) (24)26	NC	A13	NC	NC	VCC	VCC	VCC	VCC
A6	A6	A6	A6	A6	A6	A6	A6	4(2) (23)25	A8	A8	A8	A8	A8	A8	A8	A8
A5	A5	A5	A5	A5	A5	A5	A5	5(3) (22)24	A9	A9	A9	A9	A9	A9	A9	A9
A4	A4	A4	A4	A4	A4	A4	A4	6(4) (21)23	A11	A11	A11	A11	VPP	NC	WE	WE
A3	A3	A3	A3	A3	A3	A3	A3	7(5) (20)22	OE VPP	OE	OE	OE	OE	OE	OE	OE
A2	A2	A2	A2	A2	A2	A2	A2	8(6) (19)21	A10	A/O	A10	A/O	A10	A10	A10	NC
A1	A1	A1	A1	A1	A1	A1	A1	9(7) (18)20	CE	CE	CE	CE	CE	CE	CE	CE
A0	A0	A0	A0	A0	A0	A0	A0	10(8) (17)19	D7	D7	D7	D7	D7	D7	D7	D7
D0	D0	D0	D0	D0	D0	D0	D0	11(9) (16)18	D6	D6	D6	D6	D6	D6	D6	D6
D1	D1	D1	D1	D1	D1	D1	D1	12(10) (15)17	D5	D5	D5	D5	D5	D5	D5	D5
D2	D2	D2	D2	D2	D2	D2	D2	13(11) (14)16	D4	D4	D4	D4	D4	D4	D4	D4
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	14(12) (13)15	D3	D3	D3	D3	D3	D3	D3	D3

Parenthesis Indicates Pin Number of 24 Pin Packages.
24 Pin Devices are Lower Justified in Pins 3 Thru 26 of 28 Pin Socket

IV

EXTRA CONTROL

When by 1 memories are used, a single control function (chip enable), is sufficient to allow complete control over the chip's output buffers. This is because most by 1 memories have separate I/O with DATA IN and DATA OUT that are run through separate buffers whose enable controls for interfacing to common I/O busses are provided via the control functions on external bus buffers. When a bi-directional data bus is used, the need becomes much more important for an output enable ($\overline{OE}$) control function to control the time multiplexing of DATA IN and DATA OUT.

Bus contention can result without proper use of the $\overline{OE}$ control when memories are pushed to their full performance. There are ways in which interfaces between memories and their drivers can leave potential overlap in the control of the data bus. One of the most common examples of a need for independent control of the outputs when using such a fast part is during the write cycle. As shown in Figure 3, the $\overline{WE}$ control needs to be brought high t_{WPL} before the cycle actually ends. This time, equal to 50ns in the -70 parts, allows internal completion of the write cycle. After this time has elapsed, a read cycle will begin which may not be apparant to the outside world. If $\overline{CE}$ is held low for too long, a read access will occur and the memory's outputs will turn on. Since this is occurring amidst a write cycle, the opportunity exists for the memory's and the data buffer's outputs to be in contention. With an $\overline{OE}$ control this can be avoided.

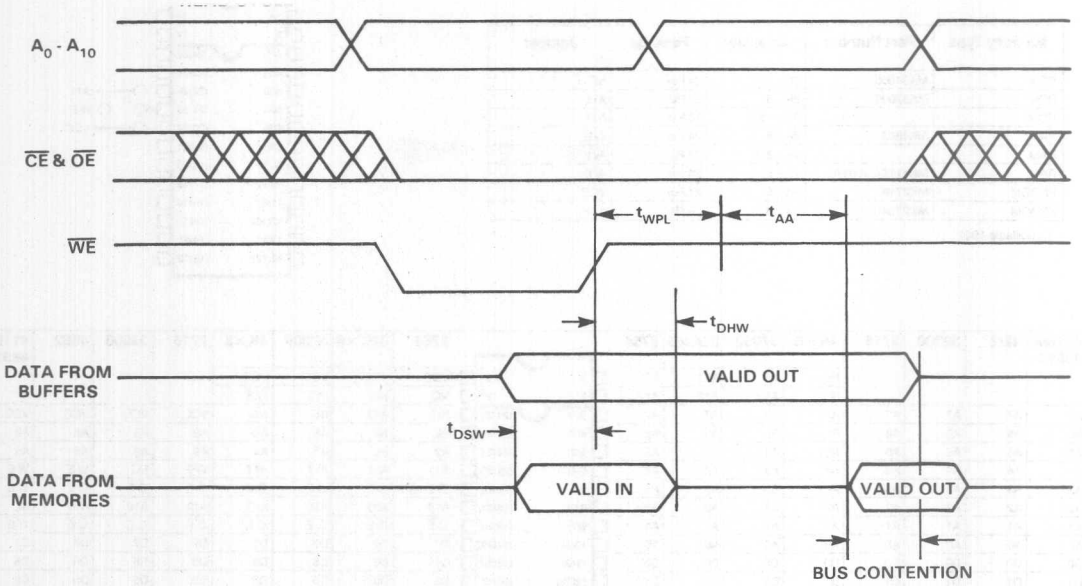
Proper system design should be able to get around this type problem, but that 50ns t_{WPL} is a maximum over the temperature range with no minimum specified. Bus contention can be something which is a function of particular ICs interacting together, and is very difficult to analyze. Also, when these output buffers begin to fight they tend to bother neighboring circuitry. Current peaks the order of 400ma due to short circuits tend to couple to other traces and if a false signal coupled to something like the $\overline{CE}$ lines, a difficult soft error debug problem lies ahead.

High speed memory design relies on predictable performance and since minimum access times are not specified, having $\overline{OE}$ control capability is necessary for a worst case design to provide for trouble-free system manufacturing.

LAYOUT

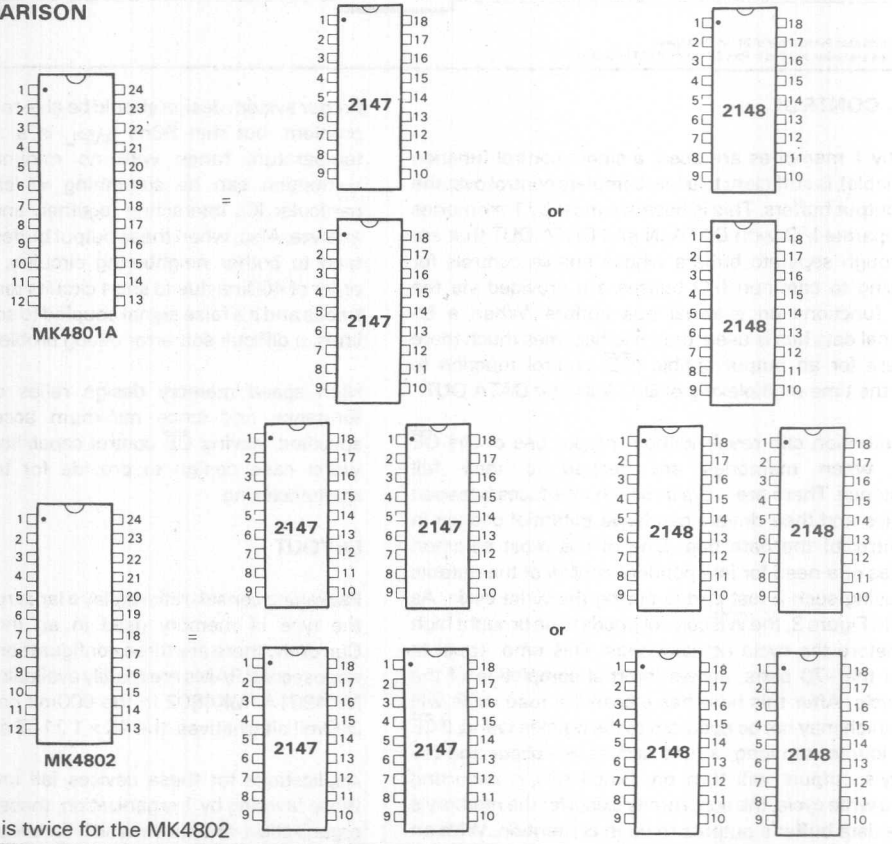
Packaging considerations play a large role in the selection of the type of memory used in an individual application. Currently, there are three configurations in which sub-100 nanosecond RAMs are readily available. Figure 4 shows the MK4801A/MK4802 in the 600mil package with the two 300mil alternatives, the 4K x 1 2147 and the 1K x 4 2148.

Applications for these devices fall into three categories, those favoring by 1 organization, those favoring wide word organization, and those which lie between the extremes.



DENSITY COMPARISON

Figure 4



P.C. Board density is twice for the MK4802

When a memory array's organization is shallow but wide, the wide word devices have layout advantages over the by 1 devices. Consider an application which could accept either memory type. The designer of a high speed 4K x 32 buffer memory can use 32 4K x 1 memories, or 16 1K x 8 devices. If the 2147 type by 1 is selected, then a layout difficulty will result. The designer could run a string of 32 devices in a row, matching the 4K x 32 nature of the array, but that will result in an overdrive condition for a single address buffer. Since square arrays provide better packaging and give short P.C. traces, the designer will probably lay the array out as shown in Figure 5, with 4 rows of 8 devices each. Compare this to the way in which the by 8 MK4801A will pack in a 4 by 4 array. A number of layout advantages exist for the by 8 array. The simple fact that there are half the chips cuts down the number of required address and control drivers. If the board is designed with rules requiring 1 driver per 8 inputs, the by 1 array will need 4 sets of 14 drivers, twice the number needed in the by 8 arrays. Also, the by 8 array takes better advantage of the data buffers with 4 memories per driver versus 1 memory per driver in the by 1 array.

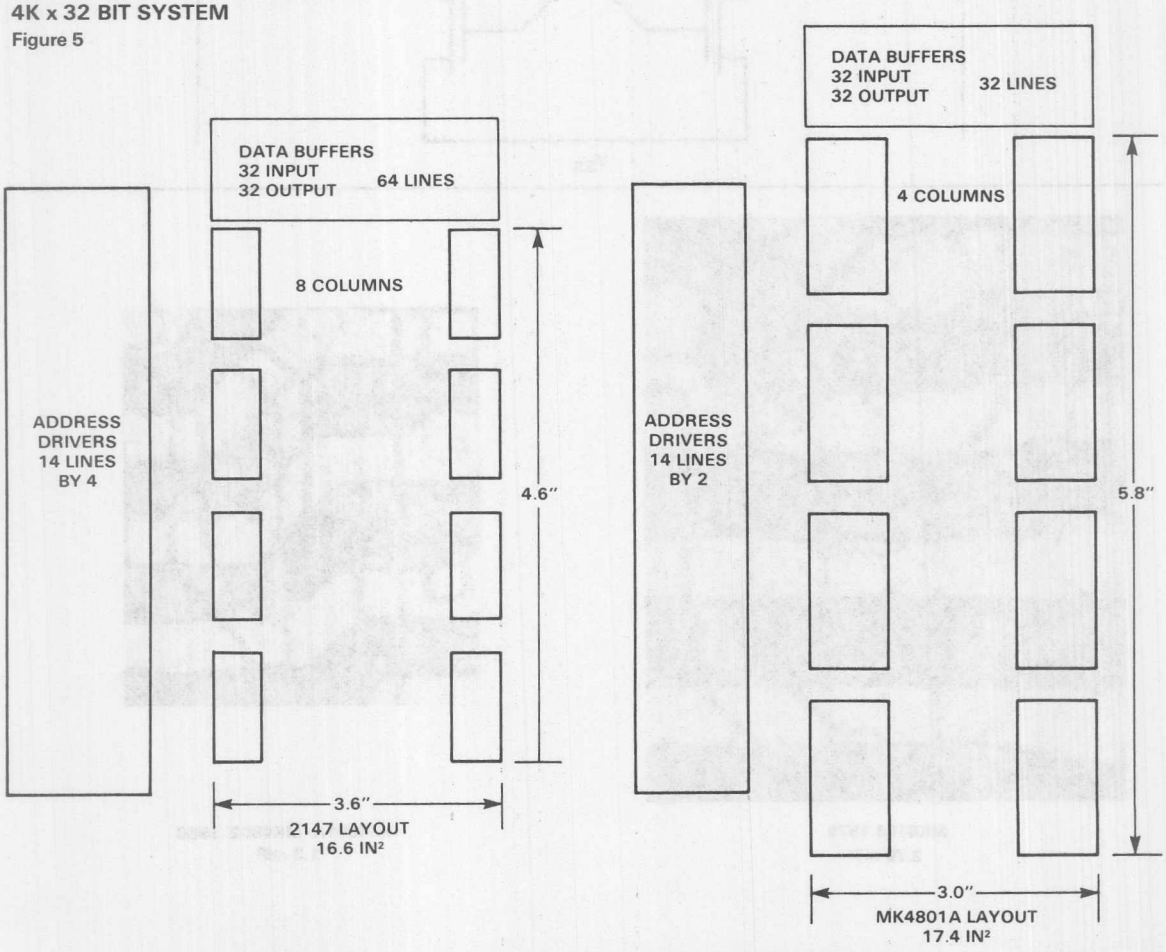
Limitations with the amount of room for P.C. traces also enter into the picture. With a single column of the by 1 array, 4 DATA IN and 4 DATA OUT lines must be run to the data I/O buffers, which are just too many to fit into the space provided. Therefore, in a realistic system, either more space must be provided, or a multi-layer card must be used for the by 1 type devices.

So where does the 2148 type device fit into this picture? As a wide word device (1K x 4) any argument which applies to a by 4 device also applies to a by 8 device. However, with equivalent packing densities in the 2148 versus the MK4801A, the by 8 devices carry the wide word advantage to the byte level. This has advantages as densities increase. If the preceding comparison looked at the 16K MK4802, the packing density would be twice that of the 18 pin devices.

DEVICE OPERATION

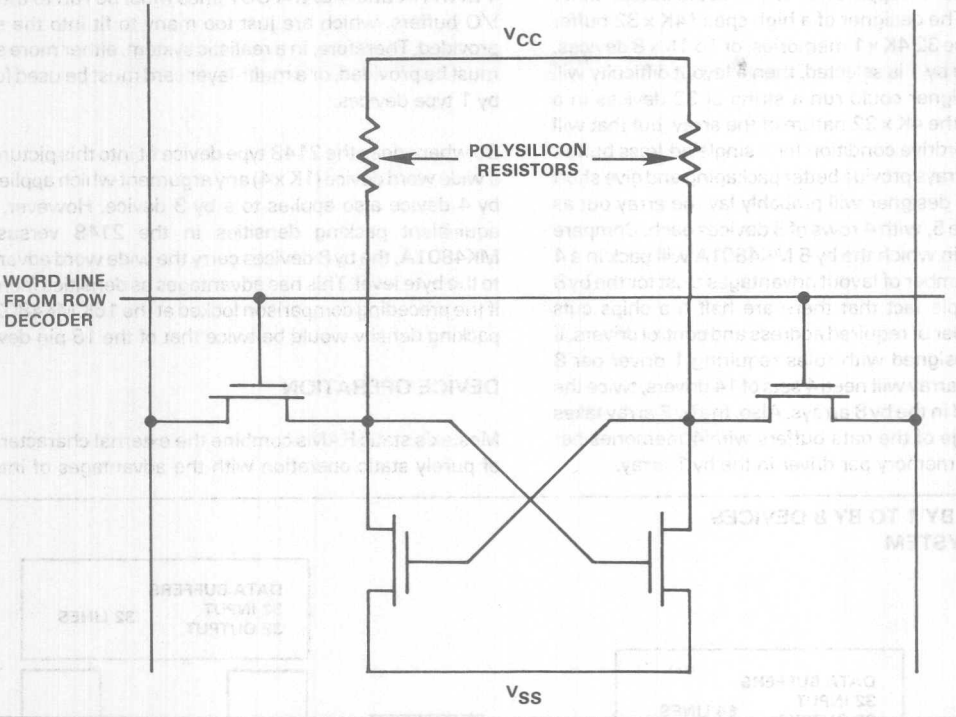
Mostek's static RAMs combine the external characteristics of purely static operation with the advantages of internal

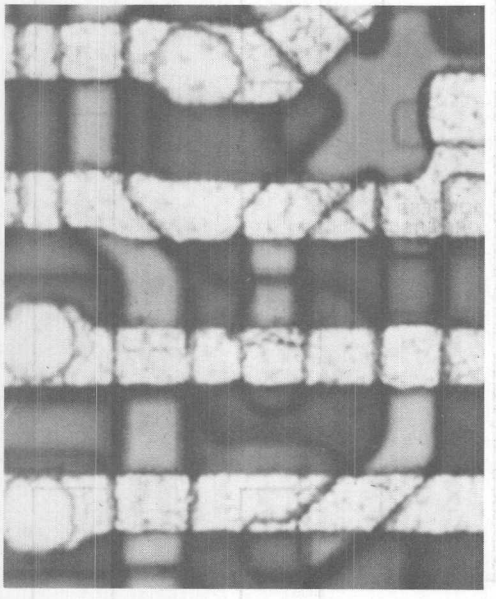
COMPARING BY 1 TO BY 8 DEVICES
4K x 32 BIT SYSTEM
Figure 5



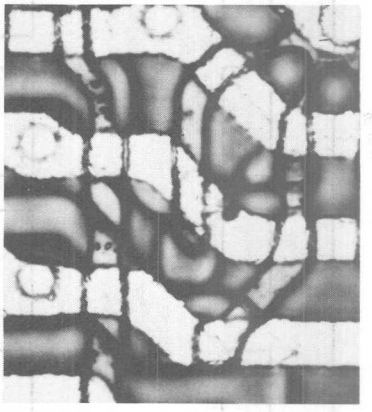
POLYSILICON STATIC RAM CELLS

Figure 6





MK4104 1976
2.75 mil²



MK4801A/MK4802 1980
1.3 mil²

dynamic periphery on the chip. The static cell used in the MK4801A/MK4802 is becoming a standard in the industry, following its introduction in the 4K x 1 MK4104 back in 1976. By employing polysilicon resistors instead of depletion load transistors, the MK4104 achieved a drastic reduction in cell size and cell power dissipation. Dimensional scaling along with processing and layout improvements have allowed the static cell to be reduced to 1.3 square mils. Figure 6 shows the comparison between cells, along with the cell's schematic diagram.

The peripheral circuitry surrounding the memory matrix is where the dynamic nature of the chip enters in. Clocked sense amps and clocked decoder circuits provide fast N-channel MOS performance without consuming large amounts of steady state power. Figure 7 shows an oscilliscope photo of the current consumption in a MK4801A. Here, peak currents of 136ma were measured during the cycle, with the DC paths in the part only consuming 36ma. The resulting average I_{CC} current is much less than the data sheet specification of 125ma, however lower temperature operation and processing variations will affect the "typical" average I_{CC} consumption as the process is optimized for speed.

Read and write cycles operate under different system considerations, and Mostek has developed these memories to recognize this fact. The result is a ripple through read, and an Edge Activated™ write cycle.

ADDRESS ACTIVATED™ READ

Read cycles operate in a completely static mode; they require no external clocks for proper operation. A true ripple through operation results from an address change. The photo in Figure 7 shows changes in DATA OUT in response to an address change only; the control signals remained low. Referring to the internal logic diagram of Figure 8, all address lines feed into buffers which generate a SAT pulse. It is the trailing edge of this pulse which initiates the Ø1 clock shown in the figure. This pulse, for Sense Address Transition, is generated whenever any of the address lines change logical states. It is the SAT detectors which allow these RAMs to appear completely static in the read mode.

These timing diagrams show two different types of access times. The t_{AA} shown in the timing diagram of Figure 9 reflects the full rated speed of the part. This means that the fastest access is initiated upon address transitions and is measured from the time at which the last address line is stable. The other two times, t_{CEA} and t_{OEA}, are equal to half of t_{AA}. Referring to the logic diagram of Figure 8, it can be seen that when $\overline{WE}$ is high, the only effect that $\overline{CE}$ and $\overline{OE}$ have is upon the buffer and in the read mode this is the only function for both the $\overline{CE}$ and the $\overline{OE}$ controls.

Data appears at the output via a rather straightforward procedure. There are eight arrays of 128 x 8 cells each representing one of the eight parallel outputs. Seven of the address lines feed into a row decoder which selects one of 128 rows (for the MK4802, there are 256 rows, one of which is selected by 8 of the address lines). Then all eight cells in each row dump their data onto the metal data and $\overline{data}$ lines running the length of the array. The three remaining address lines feed into a column decoder which then select one of eight sense amps at the top of each memory matrix. It is the fact that the data and $\overline{data}$ lines are low resistance metal which allows the MK4801A to be doubled to produce the MK4802 while keeping the same data sheet specs. Propagation delays along these metal lines (which are double in length) are short compared to the more resistive polysilicon row lines (which keep the same length) which feed the outputs of the row decoder into the array.

On the trailing edge of the Ø1 clock, the selected sense amp will provide drive to the output buffer. Assuming that $\overline{CE}$ and

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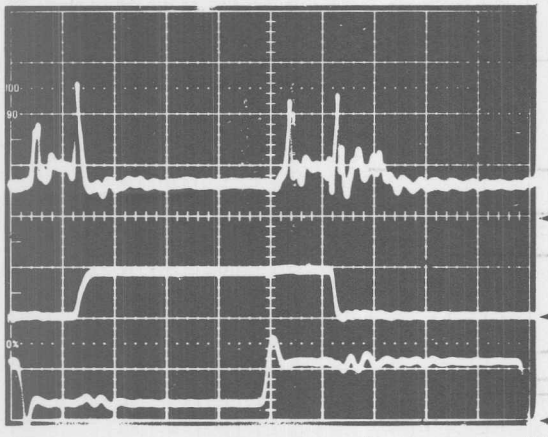
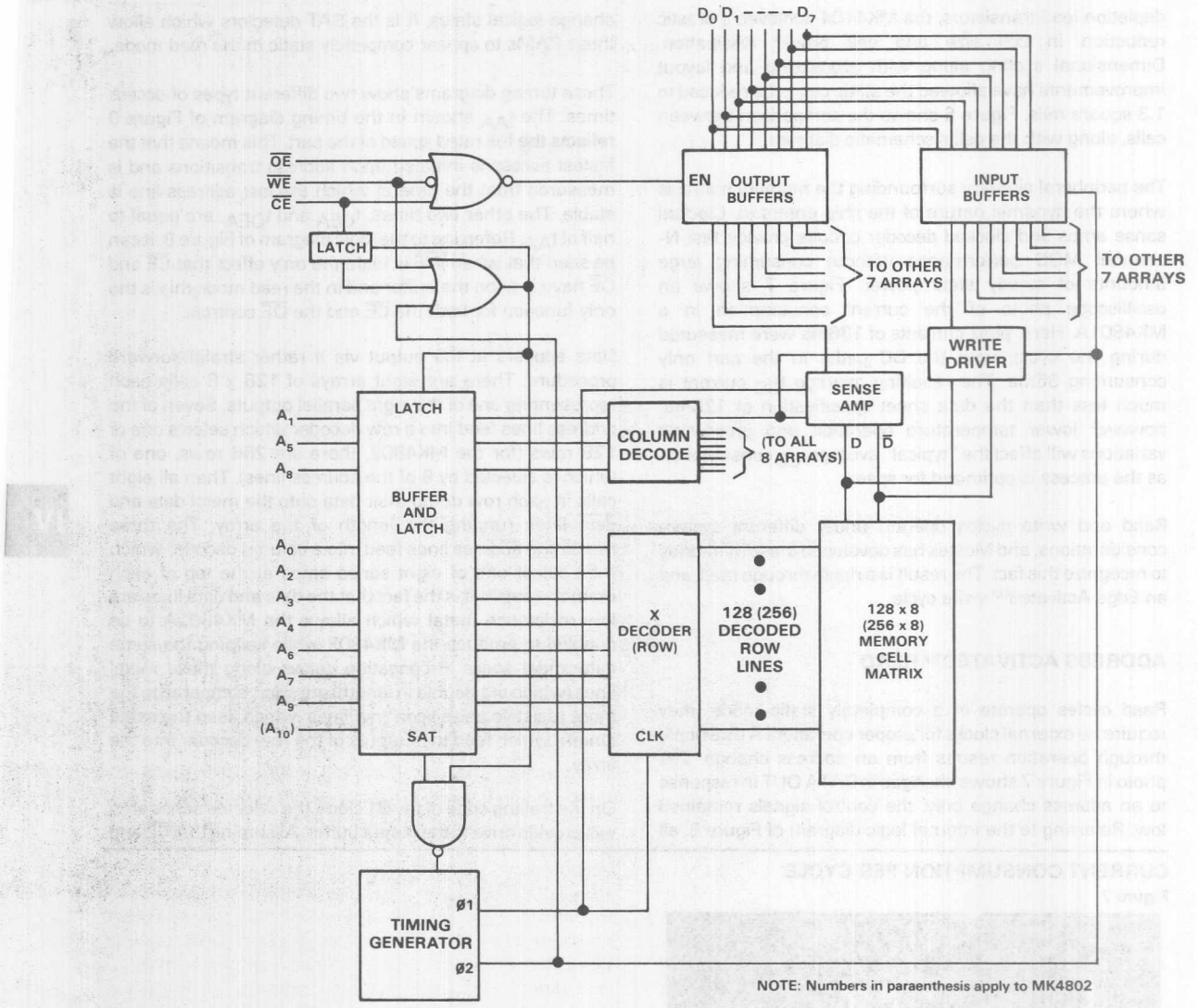
CURRENT CONSUMPTION PER CYCLE

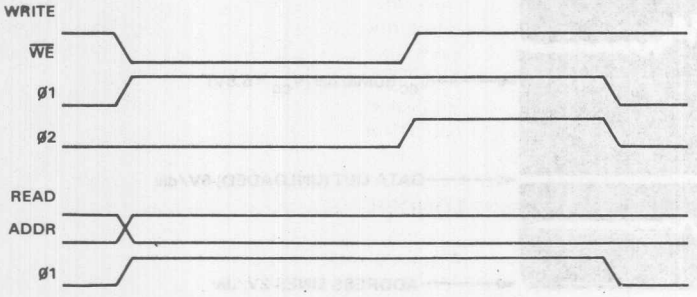
Figure 7



Device operating at 250ns period
Fully static reads accessing in ~ 70ns (OE = CE = O)

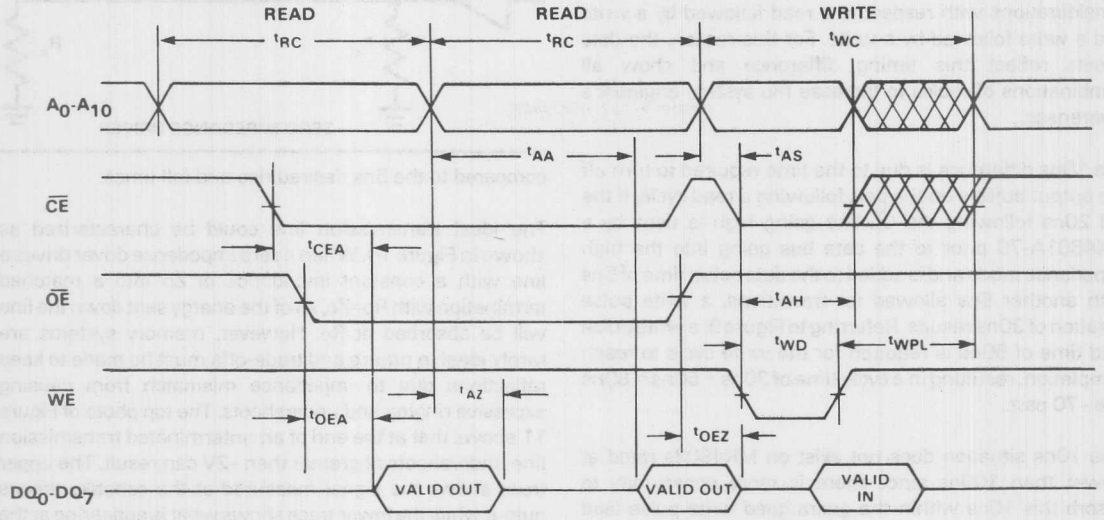


NOTE: Numbers in paraenthesis apply to MK4802



TIMING DIAGRAM

Figure 9



IV

$\overline{OE}$ have been brought low within their access times, a single transition will occur at the outputs from the high impedance state to valid data. It should be noted that while Ø1 is active, the output buffers are disabled, guaranteeing a high impedance output. When address transitions occur before the completion of the access, the Ø1 cycle will not be completed, a new access will begin, and the outputs will remain in the high impedance state.

The advantage of an address activated read cycle is basically one of speed. As any system application would show, time is required to decode some of the highest order address lines into the $\overline{CE}$ signal. If chip access time begins from address transition instead of from the edge of $\overline{CE}$, then the chip decode time no longer needs to be minimized allowing the use of slower logic while speeding up system operation.

EDGE ACTIVATED™ WRITE

The consideration alluded to earlier causing the write cycle to operate differently from the read is basically one of data security. System noise during a read may abort a cycle, but it will not cause loss of data.

A simple example shows this need. If a write cycle were to operate the same as a read, and noise coupled into one of the address lines halfway through the Ø1 period, the write would be aborted potentially leaving the 8 cells in indeterminate states. So protective measures have been taken on the chip to eliminate this possibility.

Referring again to Figure 8, as soon as both $\overline{WE}$ and $\overline{CE}$ become active a signal is generated which latches up the status of the address inputs. It also marks the beginning of the familiar Ø1 clock. For a time referred to as t_{WD}, the row and column decoders are selecting the cell in each matrix to be written into and for t_{DSW} the data present at the I/O port is settling in the input buffers. When $\overline{WE}$ goes from low to high, the actual write process begins. At this point the Ø2 clock goes active preventing any activity on $\overline{CE}$ or $\overline{WE}$ from interfering with the completion of the write cycle. The Ø2 clock also enables the write drivers, which force the data and $\overline{data}$ lines for the selected column line to the cell input transistors, writing the cell. Then at the completion of Ø2, both Ø1 and Ø2 go low, allowing the start of a new cycle.

LONGER WRITE

A quick glance at the data sheets reveals that for the -55, -70, and -90 parts, the write cycle is rated at 65ns, 80ns,

and 100ns respectively. This 10ns difference between the read and write cycles reflects realistic system constraints. Inside the parts, access time is determined by the Ø1 clock, which is the same for both types of cycles. However, a bi-directional data bus imposes some important timing considerations with respect to a read followed by a write and a write followed by a write. For this reason, the data sheets reflect this timing difference and show all combinations of cycles to increase the system engineer's awareness.

The 10ns difference is due to the time required to turn off the output buffers on the part following a read cycle. If the full 20ns following the $\overline{CE}$ line going high is used by a MK4801A-70 prior to the data bus going into the high impedance mode and is added to the data setup time of 5ns with another 5ns allowed for transitions, a write pulse duration of 30ns results. Referring to Figure 9, a write pulse lead time of 50ns is required for the write cycle to reach completion, resulting in a cycle time of 30ns + 50ns = 80ns in a –70 part.

This 10ns situation does not exist on MK4802s rated at slower than 100ns since there is more opportunity to absorb this 10ns within the guaranteed write pulse lead time t_{WPL}. In fact, on the MK4802-1 and the MK4802-3, $t_{WP} + t_{WPL}$ do not add up to t_{WC}, but add up to 10ns less.

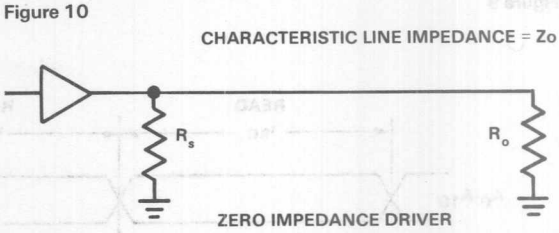
Success in designing high speed memory systems is closely tied to the attention given to analyzing delays through peripherials and other timing problems on the order of 5ns or 10ns. When such short times are of importance, transmission line effects start to enter into the picture and need to be considered as such to obtain the maximum system importance.

DRIVING AND TERMINATING

As system speeds increase, the design of the memory interface becomes much more than simply picking up an IC manufacturer's data book and selecting parts. Cycle times below 100ns require that every nanosecond available be usable by the parts, and not eaten up in propagation delays and ringing. In order to keep this wasted time to a minimum, a basic appreciation for the behavior of high frequency signals on a P.C. board needs to be obtained and this behavior needs to be accounted for.

When the propagation delay of an interconnection becomes significant with respect to the rise and fall times of the driver, the circuit enters the realm of transmission lines. If these effects are not considered, soft errors resulting from noise are possible. Some of these effects were looked at on a memory board which had been designed to exercise these memories. This was a 4 layer P.C. board with internal power and ground planes employing .020 line and spacing rules. Propagation delays of around 4 nanoseconds per foot were measured on this board, and since a row of 16 devices is 12 inches long, the propagation delays encountered are large compared to the 5ns desired rise and fall times.

IDEAL TRANSMISSION LINE
Figure 10



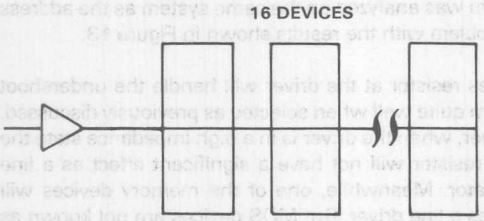
The ideal transmission line could be characterized as shown in Figure 10. When a zero impedance driver drives a line with a constant impedance of Zo into a matched termination with Ro=Zo, all of the energy sent down the line will be absorbed at Ro. However, memory systems are rarely ideal in nature and trade-offs must be made to keep reflections due to impedance mismatch from causing excessive ringing and undershoots. The top photo of Figure 11 shows that at the end of an unterminated transmission line undershoots of greater than –2V can result. The upper trace shows the signal measured at the schottky drivers output while the lower trace shows what is appearing at the end of the line. Mostek places a specification of –1.5V (for less than 50ns duration) as the minimum voltage on any pin, which this exceeds. However many manufacturers place a specification of –0.3V or –0.5V on undershoot. That makes proper termination all the more crucial.

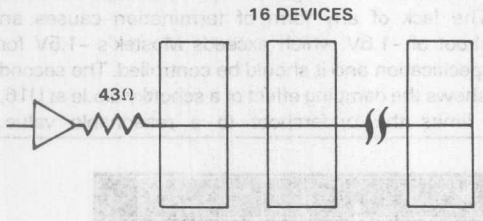
There are three commonly used techniques to rectify the undershoot problem. One of the simplist is a series resistor which serves to match the source impedance of the driver to the impedance of the P.C. trace. The second photo of Figure 11 demonstrates how well a 43Ω resistor attenuates that large undershoot found in the P.C. trace of the upper photo. Not only was the undershoot reduced but the noise on the line was also reduced without much degradation of the waveform. However since the PC trace has a characteristic impedance of around 80Ω some slight undershoot still results. The value of the series resistor can be empirically selected, however too large a resistor value will eliminate the undershoot at the expense of transition time and noise immunity.

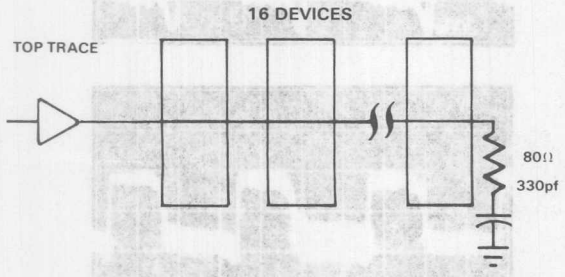
A second termination technique shifts the problem from the driver to the receiver. The series resistor used earlier is a form of reverse termination, allowing a single bounce from the impedance mismatch found when the PC trace ends. By properly terminating the end of the line, no reflection will occur resulting in a clean signal. But a simple 80Ω resistor placed at the end of the line presents an excessive DC load on the driver. Therefore, a capacitor is placed in series, allowing an AC termination into Zo and a DC open circuit to reduce loading. As can be seen in the third photo of Figure 11, undershoot is controlled on the line but the capacitor used is larger than may be required, restricting rise times. As suggested for the series resistor, R and C values can be selected empirically.

DRIVING THE ADDRESS BUS

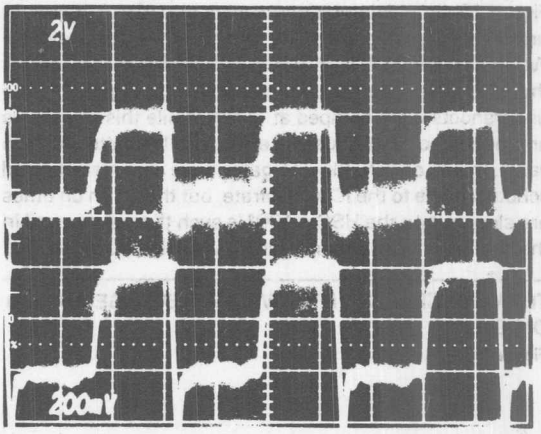
Figure 11

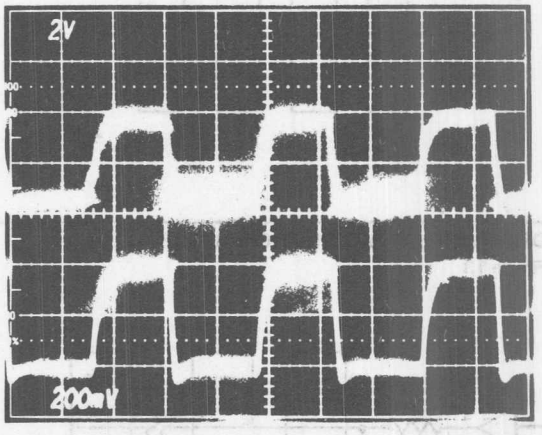


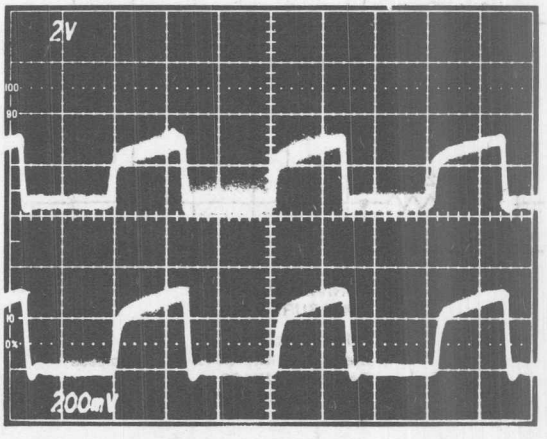




Vertical 2V/div
Horizontal 50ns/div







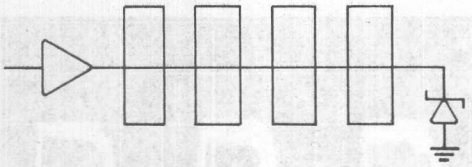
Driver - 8T97
Memories - MK4801A-90 16 pieces
Resistors - carbon composition
Capacitor - mica

IV

Schottky diodes are also used as line terminators, although they handle the problem of undershoot in a more "brute force" manner. A forward biased schottky diode begins conducting at 0.3V, so a schottky diode placed as shown in Figure 12 should damp undershoots at –0.3V. But greater undershoots result due to the turn on times of real diodes. When a Hewlett Packard HSCH-1001 diode was placed at the end of the line used for the photos of Figure 11, the undershoots were damped at –1.0V. While this still leaves an undershoot, the diode will effectively limit it to a known value. Inputs on schottky TTL gates have a reversed biased schottky diode to the IC's substrate, but their turn on times are slower than the HSCH-1001's such that when used in the same example the undershoot was clamped at –1.6V.

TERMINATING THE LINE WITH A REVERSE BIASED DIODE

Figure 12



DRIVING THAT BIDIRECTIONAL BUS

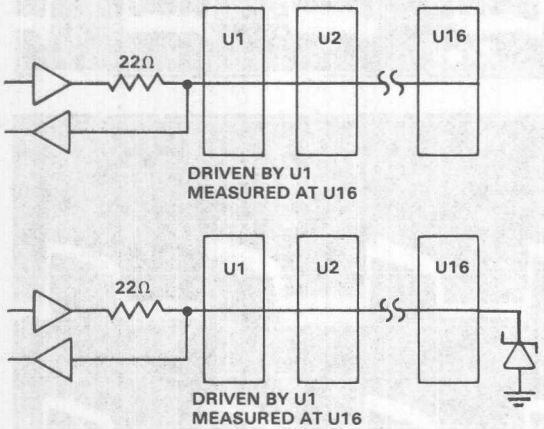
When considering the transmission line nature of a trace on a PC board, the example of a bidirectional data bus becomes very interesting. Not only is there a situation similar to a single driver driving a number of memory inputs, but each memory itself drives the line during a read cycle. This problem was analyzed on the same system as the address bus problem with the results shown in Figure 13.

A series resistor at the driver will handle the undershoot problem quite well when selected as previously discussed. However, when the driver is in a high impedance state the series resistor will not have a significant effect as a line terminator. Meanwhile, one of the memory devices will serve as a line driver. But MOS devices are not known as powerful line drivers and cannot compete for speed or low impedance when compared with a Schottky TTL device.

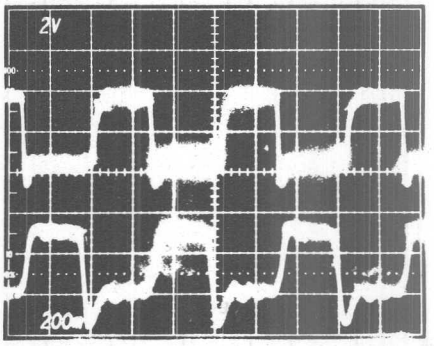
The scope photos in Figure 13 all show the address line in the upper trace which causes a read cycle to commence ($\overline{CE}$, $\overline{OE}$ low, $\overline{WE}$ high). The lower traces show the data line with the part operating at near its maximum speed (data transitions at or near the following address transition). The two photos have U1 driving the line, measuring the trace at U16. The lack of any form of termination causes an undershoot of –1.6V which exceeds Mostek's –1.5V for 50ns specification and it should be controlled. The second photo shows the damping effect of a schottky diode at U16, which limits the undershoot to a reasonable value.

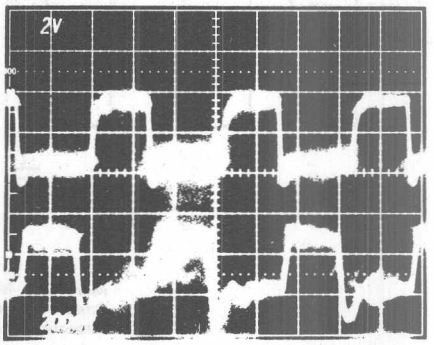
DRIVING THAT BIDIRECTIONAL BUS

Figure 13



Driver - 74LS244
Memories - MK4801A-90 16 pieces
Receiver - 74S153
Diode - HDSP 1001





Alternate terminations prove to be undesireable for the bidirectional bus. Series resistors at each device require excessive real estate, and a RC termination excessively loads down the MOS drivers.

PC LAYOUT - PLANNING AHEAD

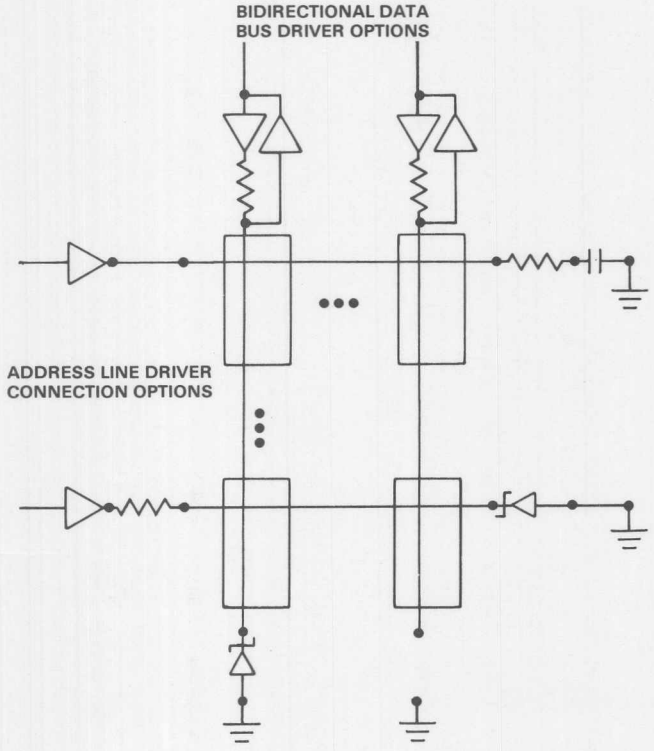
The choice of the type of termination, and the values to be used, depend on many variables. A limited number of these choices are viable options but the characteristics of printed circuit board traces vary enough that the selection of a specific combination of terminations should be delayed until a prototype can be characterized. If the resultant combination gives excessive undershoot or sluggish rise times, the selected values can be changed. Following are some suggestions for terminations, and Figure 14 shows a generalized memory array using these techniques.

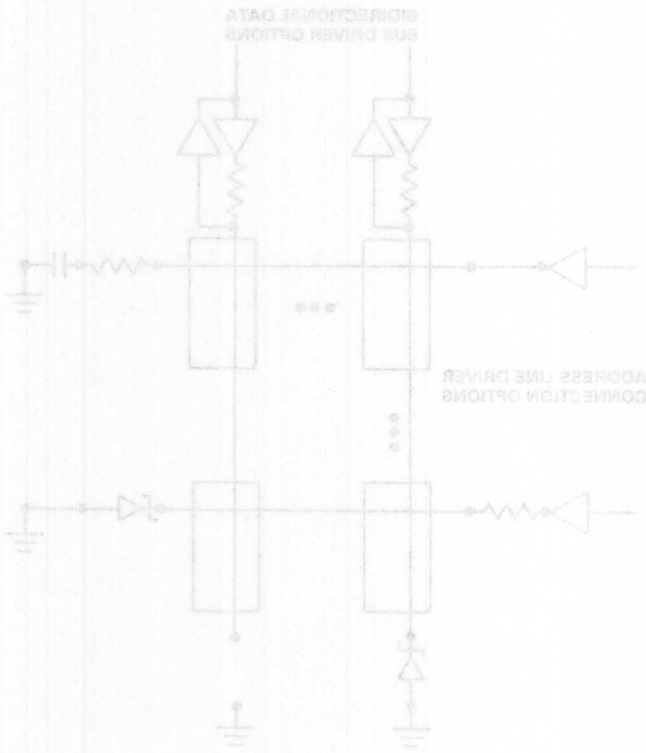
1) Provice a series resistor in the address and control lines. Also provide for a R-C high frequency shunt at the end of the trace should it necessary. Generally one or the other of these will be selected.
2) Provide a series resistor at the data driver, but not between the data line and the receiver. When the resistor is between the data line and the receiver, the IR drop substracts from the noise margin. Also provide for a schottky diode at the end of the data line to provide termination when one of the memory devices is driving the line.

CONCLUSION

System designs can easily take advantage of the Bytewyde nature of the MK4801A/MK4802, but no system design in the sub 100ns speed is done without a high degree of care. Proper selection and design of the peripheral circuitry and proper layout of the array keeping traces short are vital to assure consistant performance, and these RAMs have been designed to make it easier. The wide word format, fast circuit operation, output enable control, Address Activated™ read, Edge Activated™ write, and ability to withstand -1.5V undershoots serve to make that system design easier. Cost has also been factored into the situation by virtue of the small die size. As manufacturing experience accumulates on these parts, a classical price reduction should occur making the MK4801A and the MK4802 more than competitive in the marketplace.

DESIGNING PC BOARDS WITH TERMINATOR OPTIONS
Figure 14





1982/1983 MEMORY DESIGNERS GUIDE

MOSTEK®

PRODUCT ENHANCEMENT

Reliability Report

V

RELIABILITY

V

RELIABILITY

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RELIABILITY

The terms "Quality" and "Reliability" are often misused, confused and misinterpreted in today's semiconductor industry. Quality has found use as a measure of the relative worth of things with terms such as "good quality" or "bad quality" in widespread use. However, quality is simply conformance to requirements. A quality semiconductor device is then one that meets or exceeds its published specification. Reliability then becomes a measure of how well a quality device will perform to the specification over time.

Reliability is certainly not a new buzz word. But, reliability, or the lack of it, has taken on increased importance in the MOS memory market. In the 80's, due to increasing memory requirements, people will find it advantageous to package as much memory as feasible, in as small an area as possible. This ever increasing complexity will require improved device reliability in order to maintain system reliability at acceptable levels.

To meet the challenge of the 80's, Mostek has established a number of programs to define product reliability levels. Among these programs are 1) the qualification of new products, processes and packages, 2) the Product Monitor Program (PMP) to monitor current product reliability and 3) the reduction of current failure rates through a program of failure analysis and feedback.

QUALIFICATIONS

The procedures for qualification of all new devices require design reviews, documentation and characterization. After careful evaluation of all engineering studies, a formal device qualification is performed and the product is ready for presentation to the marketplace.

Qualification of all new processes follows a path similar to that of all new devices. However, additional participation of the Quality Control Department is required to insure that the necessary QC test procedures are in place for the new process. Any significant modification to any existing process is treated as a new process for the purpose of qualification.

New packages are qualified and released for production after having successfully completed all prescribed environmental tests. Again, any significant modification to any existing package or packaging material is treated as a new package for the purpose of qualification.

RELIABILITY

After successfully completing qualification, the new product, process or package is ready for presentation to the marketplace. Mostek's qualification process insures quality products. The question then arises as to how long will the product perform to specification or how reliable is the product.

Reliability can be greatly impacted by proper design techniques. Consider the effect of power dissipation upon the reliability of two 16K RAMs, one dissipating 900 milliwatts and one dissipating 450 milliwatts while operating at 70°C.

$$T_J = T_A + (\Theta_{JX} \bullet P_D)$$

where

T_J is the junction temperature
T_A is the ambient temperature
Θ_{JX} is the junction to ambient thermal resistance (this value is 70°C/Watt for a 16 pin ceramic DIP mounted in a socket on a double-sided PC board)
P_D is the power dissipation of the device under the conditions of interest.

Then,

$$T_{J1} = 70°C + (70°C/W)\,(0.450W) = 101.5°C = 374.5°K$$

and

$$T_{J2} = 70°C + (70°C/W)\,(0.900W) = 133°C = 406°K$$

The vast majority of all MOS failure mechanisms are accelerated by temperature. The rate of acceleration is predicted by the Arrhenius equation which can be expressed as,

$$R = R_0 \, EXP\left(-\frac{E_A}{KT}\right)$$

where

R is the reaction rate
R_0 is a constant
E_A is the thermal activation energy in electron volts (eV)
K is the Boltzmann's constant (8.63×10^{-5} eV/°K)
T is the temperature in degrees Kelvin (°K)

V

Rewriting the equation to allow a comparison of reaction rates at two different temperatures T_1 and T_2 we have:

$$\frac{R_2}{R_1} = EXP\left[\frac{E_A}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right]$$

Now the effect of power dissipation on reliability can be evaluated. Substituting T_{J1} and T_{J2} (in °K) into this equation and assuming that E_A = 1.0 eV, we arrive at

$$\frac{R_2}{R_1} = EXP\left[\frac{1.0}{8.63 \times 10^{-5}}\left(\frac{1}{374.5} - \frac{1}{406}\right)\right]$$

$$\frac{R_2}{R_1} = 11.03$$

which predicts a failure rate for the 900 milliwatt device of about eleven times that of the 450 milliwatt device, due to the 31.5°C difference in junction temperature.

PRODUCT MONITOR PROGRAM

The PMP or Product Monitor Program monitors reliability on current products on an on-going basis. A variety of devices and packages are selected for this program. All stress testing is done according to the applicable methods of MIL-STD-883B or Mostek standard in cases where no military standard is available. Table 1 lists some of the stress tests performed on the Product Monitor Program.

STRESS TESTS PERFORMED

Table 1

Test	Standard	Stress
High Temperature Dynamic Operation	MIL-STD-883B M 1005 Cond. D	125°C
Temperature Cycling	MIL-STD-883B M 1010 Cond. C	-65°C/+150°C
Thermal Shock	MIL-STD-883B M 1011 Cond. B	-55°C/+125°C
Hermeticity	MIL-STD-883B M 1014 Cond. B and C Hermetic packages Only	
Solderability	MIL-STD-883B M 2003	260°C, 10 sec.
Lead Integrity	MIL-STD-883B M 2004 Cond. B2	
Constant Acceleration	MIL-STD-883B M 2001 Cond. E Hermetic Packages Only	30 Kg., Y1 Plane
85°C/85% RH	Mostek (Plastic Only)	85°C/85% RH 1000 Hours

In addition to the Product Monitoring Program, the "Monitored Memory Program" provides soft error failure rates. Devices are operated in a simulated system environment chosen to represent typical use conditions. These conditions include nominal operating supply voltages, nominal timing and an ambient temperature of approximately 40°C. Data outputs are monitored during each read cycle to provide soft error data. This second program also provides actual "hard" failure rates which can be compared to the derated 125°C operational life test results.

TESTING

Probably the most obvious problem associated with testing memories is that of test time. Some common industry patterns with their appropriate test times for a 4K, 16K and 64K RAM are shown in Table 2.

COMMON INDUSTRY TEST PATTERNS

Table 2

Pattern	# Of Cycles	Test Time (Cycle Time = 375 nS)		
		N=4096 Bits (seconds)	N=16384 Bits (seconds)	N=65536 Bits (seconds)
Checkerboard	4 N	$6x10^{-3}$	$25x10^{-3}$	$98x10^{-3}$
Galloping Columns & Rows	$4 N^{3/2}$	$98x10^{-9}$	3	25
Walkpat	$2 N^2$	13	201	3221
Galpat	$4 N^2$	25	403	6442

The test times listed assume only one pass testing. Most RAMs still have three power supplies yielding eight combinations of power supply limit conditions. Different timing sets and temperatures adds additional combinations and increases the test times accordingly. However, an effective yet short test plan can be developed by shifting the burden from test time to the initial characterization plan. An in-depth characterization plan will show the device parameters that have the highest potential for causing problems in a particular memory system design. It will also show which parameters appear to be most likely to drift out of specification as part of the device's inherent parametric distribution. Also, it is required that the device design be one that is not sensitive to a wide variety of complex test conditions. In this way a large amount of test time can be saved and Mostek is able to effectively and economically test its memory devices and provide a quality product to the marketplace.

V

FAILURE MECHANISMS

Although the user may not choose to do extensive reliability testing himself, he should be familiar with the basic failure mechanisms and methods employed to screen them out prior to purchase. At this time, two failure mechanisms account for between 60% and 85% of all reported RAM failures. These two mechanisms are oxide defects and defects caused by foreign contamination. The screens required for the elimination of these two types of defects vary greatly.

Oxide defects are random imperfections in the SiO_2 gate oxide. These defects can be introduced during the manufacturing process and then rupture when subjected to an electric field for some period of time. This type of failure mode can be screened effectively by subjecting all devices to an overvoltage stress. The screen's effectiveness is proportional to the voltage applied (field intensity) and the time of stress. When the stress occurs is also significant. If an overstress voltage occurs during burn-in, it may last for 12 to 24 hours. However, an overstress voltage during a functional test sequence lasts less than a few seconds.

The second major category of failures are those caused by contamination of the device by some foreign impurity. These are normally mobile ions such as sodium that can move under the influence of temperature and the applied field to some point in the circuit where they result in threshold voltage shifts of the MOS devices. This failure mode is well known in the industry and is accelerated by thermal stress.

The activation energy for contamination-related failures is approximately 1.0 eV while the activation energy for oxide failures is approximately 0.3 eV. For this reason, a high temperature burn-in at 125°C greatly reduces the incidence of field failures directly related to contamination. The effectiveness of burn-in on gate oxide failures is more a function of the applied voltage than of the temperature.

FAILURE RATE CALCULATIONS

The use of life test data to calculate failure rates and predict what is likely to occur in the future or under other operating conditions, requires the use of a definable, statistical failure distribution. This mathematical model, if valid, then provides the necessary formulas to allow the user to make failure rate projections.

The most widely used and accepted distribution for describing the mean life and failure characteristics of MOS devices is the exponential distribution. However, the exponential distribution is based on two assumptions. These are 1) that only random failures occur and 2) the failure rate is constant. Because of this, the exponential distribution does not account for any variation in the failure rate. A more flexible distribution is required.

Mostek utilizes the Weibull distribution. This distribution was chosen because it presents a more realistic representation of the data. In order to use this distribution properly, enough device hours must be accumulated to generate a sufficient number of failures. As the failure rate of MOS devices becomes lower and lower, the number of device hours required increases proportionally.

When using a statistical failure model, the hazard rate (instantaneous failure rate) is defined as,

$$h(t) = \frac{f(t)}{1-F(t)}$$

where f(t) is the probability density function which gives the relative frequency of failures at a time, t. F(t) is the cumulative distribution function which gives the summation of failures proportional to that time. For the Weibull distribution,

$$f(t) = \frac{\beta}{\alpha} \cdot (t - \gamma)^{\beta-1} \cdot \text{EXP}\left[\frac{(t-\gamma)^{\beta}}{\alpha}\right]$$

and

$$F(t) = 1 - \text{EXP}\left[\frac{(t-\gamma)^{\beta}}{\alpha}\right]$$

resulting in a hazard rate as follows:

$$h(t) = \frac{\beta}{\alpha} (t-\gamma)^{\beta-1}$$

You will note that the hazard rate (instantaneous failure rate) is a function of time (t) and the constants α, β and γ.

γ is a time delay parameter and is only used when the data does not fit the distribution without its use. Since it is assumed that MOS devices are subject to failure at the moment they are put on stress, it can be assumed that $\gamma = 0$ (which has been verified experimentally). The hazard rate than becomes,

$$h(t) = \frac{\beta}{\alpha} t^{\beta-1}$$

The flexibility of the Weibull distribution can now be demonstrated by looking at various values of the constant β. When $\beta = 1$ the hazard rate becomes,

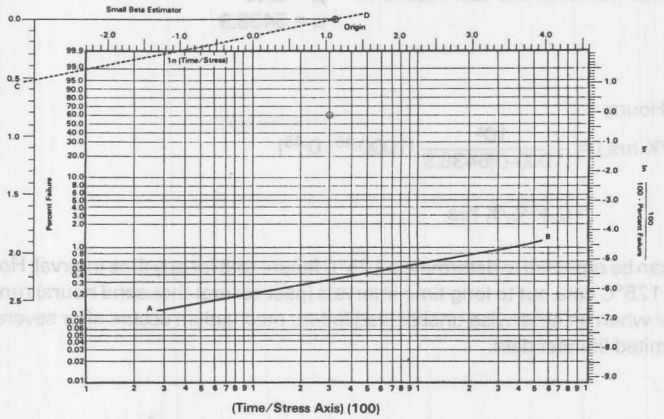
$$h(t) = \frac{1}{\alpha}$$

which is a constant failure rate and the Weibull distribution reduces to the exponential distribution. Thus, in those cases where the exponential distribution is justified, the Weibull will provide the correct results. When $\beta = 2$ we have a Rayleigh distribution and when $\beta > 3$, a Gaussian distribution is observed. In the case of MOS devices, it is most common to observe a $\beta < 1$. In this case the distribution resembles the exponential distribution but with a much steeper drop off. The constants α and β can best be understood by looking at a sample of Weibull plotting paper as shown in Figure 1.

On this paper, cumulative percent defective is plotted versus time. The constant β is the slope of this line. A line (CD), parallel to the data line plot (AB), drawn through the origin circle ⊕, intersects the left most vertical line with an approximate value of β. This should be done before a detailed analysis of the data is begun. When $\beta > 1$ the failure rate is increasing with time, indicative of a wearout situation. When $\beta < 1$ the failure rate is decreasing with

WEIBULL PLOTTING PAPER

Figure 1



time as expected with MOS devices. And, when $\beta = 1$ the failure rate is constant. Thus, by plotting the data, even before a failure rate has been determined, you can verify whether the devices are behaving as expected or an abnormal failure rate situation exists.

The constant α is a function of the Y-intercept of the data line plot

$$\ln \alpha' = - Y\ INT$$

If you look carefully at Figure 1, you will see that the X-axis is Time/Stress x 10^2 and not Time/Stress x 1. Thus, the X-axis has undergone a linear transformation. If a Time/Stress x 1 axis was used, our Y-intercept would be different and thus, also, our value of α. Therefore, we must correct our value of α by either replotting on Weibull paper having a different X-axis or by applying a linear transformation to α. Since many different Weibull papers exist, we will apply a linear transformation resulting in

$$\alpha = \alpha' (10^{K\beta})$$

where K = the degree of the linear transformation (K = 2 for the paper used in Figure 1). We now have values for both the constants β and α and a value of h(t) can be determined for any time, t.

Knowing the instantaneous failure rate h(t), allows the user to calculate the mean failure rate over any time period of interest. The mean failure rate (in %/K hrs.) from time t_1 to time t_2 is

$$FR(\%/K\ HRS) = \frac{10^5}{t_2 - t_1} \int_{t_1}^{t_2} h(t)\, dt$$

$$= \frac{10^5}{(t_2 - t_1)\,\alpha} (t_2^{\beta} - t_1^{\beta})$$

Example

Table 3 contains sample 125°C life test results.

125°C LIFE TEST RESULTS

Table 3

Read Points	48 hr	168 hr	500 hr	1000 hr
Sample Size	1000	999	998	997
Rejects	1	1	1	1
Percent Defective	.10	.10	.10	.10
Cumulative % Defective	.10	.20	.30	.40

For 0 - 1000 Hours,

$$125°C\ FR\ (\%/K\ hrs.) = \frac{10^5}{(1000-0)5438.9}\left(1000^{.45} - 0^{.45}\right)$$

$$= 0.41\%/K\ hrs.$$

This process can be repeated to determine a 125°C failure rate for any time interval. However, it must be noted that extrapolating 125°C data out to long time intervals (past several thousand hours) runs the risk of not being valid. This can occur when an otherwise unobserved failure mechanism occurs after several thousand hours but is not seen in the limited life test data.

DERATING

A common relationship exists between life testing and time-to-failure which involves the effect of temperature. It has been shown that temperature accelerates many physio-chemical reactions that lead to device failure. Other factors such as voltage or humidity may also affect the acceleration rate of some reactions. However, the effect of temperature is more widespread and better understood at this time.

The temperature effect that concerns us is that which corresponds to the Arrhenius equation which relates reaction rate to temperature. As stated earlier, in its simplest form the Arrhenius equation can be expressed as

$$R = R_0\ EXP\ (-E_A/KT)$$

This can be manipulated to result in

$$t_{XI} = \frac{t_{XO}}{EXP\left[(E_A/K)\left(\frac{1}{T_I} - \frac{1}{T_O}\right)\right]}$$

where t_{XO} is the time to x% defective at stress test temperature (°K)
t_{XI} is the time to x% defective at use temperature (°K)
E_A is the activation energy in eV
K is Boltzmann's constant (8.63×10^{-5} eV/°K)
T_I is the use temperature (°K)
T_O is the stress test temperature (°K)

The acceleration factor (A_f) for the various failure mechanisms are then simply the ratio of t_{XI} to t_{XO}.

$$A_f = \frac{t_{XI}}{t_{XO}} = \frac{1}{EXP\left[(E_A/K)\left(\frac{1}{T_I} - \frac{1}{T_O}\right)\right]}$$

Acceleration factors for any two temperatures can be calculated in this way. A summary of the acceleration factors for three activation energies from 125°C to 70°C and from 125°C to 55°C is given in Table 4.

ACCELERATION FACTORS

Table 4

Activation Energy	Acceleration Factor	
	125°C → 70°C	125°C → 55°C
0.3 eV	4.06	6.45
0.7 eV	26.26	77.43
1.0 eV	106.53	499.40

As shown earlier, the equation for the failure rate over any time period of interest is,

$$FR\ (\%/K\ hrs.) = \frac{10^5}{(t_2 - t_1)\alpha}\ (t^{\beta}_{2} - t^{\beta}_{1})$$

where α and β are the Weibull constants and t_2 and t_1 are the time limits of interest. To derate we simply incorporate the acceleration factor (A_{fi}) into this equation resulting in,

$$\text{Derated FR } (\%/K\ hrs) = \frac{10^5}{(t_2 - t_1)\ \alpha}\left[\left(\frac{t_2}{A_{fi}}\right)^{\beta_i} - \left(\frac{t_1}{A_{fi}}\right)^{\beta_i}\right]$$

Since there are more than one failure mechanism involved, we must generate a Weibull plot for each activation energy and the derated failure rate then becomes

$$\text{Derated FR } (\%/K\ hrs) = \frac{10^5}{(t_2 - t_1)} \sum_{i=1}^{N} \left[\frac{\left(\frac{t_2^{\beta_i}}{A_{fi}}\right) - \left(\frac{t_2^{\beta_i}}{A_{fi}}\right)}{\alpha_i}\right]$$

Any variety of data can be worked in this fashion and derated to any desired temperature over any time period of interest.

FAILURE RATE DATA

Representative Monitored Memory System data for the MK4116 16K Dynamic RAM is shown in Table 5.

MONITORED MEMORY SYSTEM DATA

Table 5

Package	Devices	Device Hours	Soft Errors	Soft Error MTBF
Ceramic (P)	2880	4,346,000	1	4.3 M Hrs.
Ceramic (J)	2688	7,539,600	7	1.0 M Hrs.
Plastic (N)	2310	5,481,000	0	6.0 M Hrs.*

*60% UCL for 0 failures

The Monitored Memory System testing conditions are as follows:

1) Operating voltages - nominal supply voltages, V_{DD} = + 12.0, V_{CC} = +5.0, V_{BB} = -5.0
2) Read/Write Cycle Period - 700 ns
3) Average Cycle Time - 6.6 μs (includes read cycles and refresh cycles)
4) Data Pattern - checkerboard / checkerboard
5) Write frequency - once per day

Representative hard failure rates for a variety of Mostek products calculated using the Weibull distribution are shown in Table 6.

DEVICE FAILURE RATE DATA

Table 6

	MK4116N 16Kx1 Dyn RAM	MK4116J 16Kx1 Dyn RAM	MK4118N 1Kx8 Sta RAM	MK36000 8Kx8 ROM
Total Devices	3861	3650	709	1586
Total Device Hrs.	3,706,492	3,295,096	611,228	1,071,016
Failures	33	29	9	18
55°C FR(%/K hrs)*	0.015	0.026	0.014	0.014
70°C FR(%/K hrs)*	0.021	0.039	0.021	0.017

* Average Life (0-100K hrs.)

It should be noted that the reliability results reported in Table 6 are "raw" results. No failures have been removed or discounted due to infant mortality or because they represent freak failures. Nor have these devices seen any special burn in or pre-processing. Thus, in any application, these failure rate results present worst-case conditions. These parts were purchased from the stockroom as standard products like a customer receives them.

REDUCING THE FAILURE RATE

The reduction of current reliability failure rates is carried out through an extensive program of failure analysis, corrective action and follow-up. When it has been determined that corrective action is necessary, this information is distributed to the necessary departments to insure the continued closed loop operation of the Qualification, PMP, failure analysis and feedback cycle.

Failure analysis on MK4116 G Rev. uncovered a sensitivity to Alpha particle induced errors. This was supported by raster scan analysis which demonstrated that soft errors are randomly distributed single bit failures. This problem was overcome by enhancing the storage cell capacity, the access transistor transfer efficiency and the word line efficiency without making any design or layout changes to the device.

The MK4116 G Rev. employs a single transistor cell with the following characteristics:

Capacitor - Poly I gate, 800 Å oxide
Transistor - Poly II gate, 1800 Å oxide
Digit Line - N^+ diffusion, capacitance ratio (digit line to cell) = 20:1.

Increasing the storage cell capacity increases the charge storage capability for a given voltage. This was accomplished on the MK4116 G Prime Rev. by decreasing the capacitor oxide to 500 Å.

This decrease did not violate the field intensity guidelines since the capacitor plate does not bootstrap above V_{DD}. Reliability studies have shown the MK4116 G Prime Rev. to be a reliable product with no failures associated with the oxide changes made.

The Poly II gate oxide thickness on the MK4116 G Rev. was 1800 Å not by design intent but rather as a processing convenience. The equation for the body effect shows a linear relationship between $\triangle V_T$ and the oxide thickness. The minimum allowable threshold voltage for a transistor is set by noise considerations. It is typically 1.3 Volts with a V_{BB} of about – 3 Volts. When the transistor is turned on by a selected word line and is writing a high level into the cell from the digit line, the value of V_{BB} approaches $|V_{BB}| + V_{DD} - V_T$ effective (V_T effective for an 1800 Å gate under these conditions is about 4.5 V). An 800 Å gate oxide lowers the body effect by a factor of 1800/800 and the resultant V_T effective is then approximately 1.9 V resulting in an improved high level of (4.5 - 1.9) = 2.6 V.

Increasing the thickness of the dielectric between Poly I and Poly II reduces the poly to poly capacitance. The word line drivers are loaded by this capacitance and at the time of sensing, the word line on the MK4116 G Rev. is at 80% of its final value. The increase in the Poly to Poly dielectric allows the word line to reach 100% of its final value before sensing and effectively increases the usable signal by 25%.

A comparison of some of the parameters for the MK4116 G Rev. and G Prime Rev. are shown in Table 7.

MK4116 G/G PRIME COMPARISON
Table 7

	MK4116G	MK4116G Prime
Capacitance Ratio (Digit Line:Cell)	20:1	14:1
Word Line Efficiency	0.8	1.0
Access Transistor Threshold (V)	4.5	1.9
Q low (Picocoulomb)	5.1	14.24
Delta V (V)	0.255	1.017
Useable Signal (V)	0.098	0.479
Electrons of Margin	6×10^5	3×10^6

One of the most significant differences is in the electrons of margin between the two revisions. Since a 5 MeV alpha particle generates 1.47×10^6 electron/hole pairs it is not until you look at the G Prime revision do you find enough margin to overcome this problem. Subsequent reliability studies have confirmed the major reduction in soft errors on the MK4116 G Prime Rev.

CONCLUSION

The Quality and Reliability of Mostek products is a function of all of Mostek. Only through strict adherence to incoming, internal and outgoing specifications can a controlled product be produced. Then, when a problem is encountered, it can be quickly analyzed and a solution effected. As failure rates continue to decrease, sample sizes will continue to increase to provide meaningful reliability data. In this way, Mostek is firm in its commitment to continue to provide quality and highly reliable products to the marketplace.

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ABSTRACT

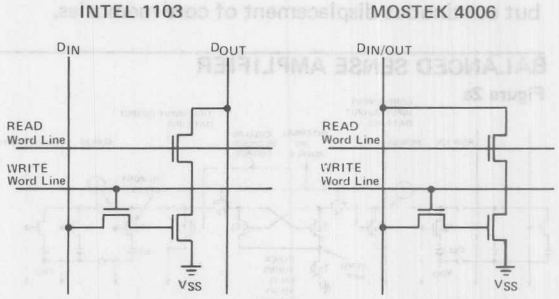
In the past decade the computer industry has witnessed the introduction and domination of the MOS RAM. Technology changes from PMOS to NMOS occurred with storage mechanisms going from 3 elements to 1. Density, correspondingly improved by a factor of 16 times while performance improved by a factor of 2. In this time frame devices evolved from complex interface requirements to simple TTL circuitry. These remarkable performance/density improvements were achieved with clever process and design innovations. Techniques used in the past have reached their limit with ROM at 64K, dynamic RAM at 16K and static RAM at 8K. A new technology will need to emerge to permit further density improvements for the future. Process and design techniques of the past and future will be discussed with attention paid to products and applications they will serve and create.

INTRODUCTION

The first density increment of MOS RAM to gain wide acceptance in the computer industry was the 1K device. The 1K device utilized P-Channel MOS technology due to the more tolerant nature of the process. Unlike its predecessors the 64 and 256 bit RAM, the 1K devices incorporated all decoding circuits on the chip. The 1K market was dominated by the 1103 from Intel and the 4006 from MOSTEK. The 1103 and 4006 were both dynamic memory devices using a small capacitor to temporarily store data. This storage technique required a periodic refreshing to retain data. The 1103 required high level clocks and complex timing considerations while the 4006 was designed for TTL compatibility and minimal timing requirements. The 1103 became the dominant part and was still being consumed in volume last year. The 4006 pinout was used by a static RAM of 1K bits. This device generically known as the 2102 has enjoyed enormous usage.

The 1103 and 4006 utilized a three transistor cell for bit storage. These cell configurations are illustrated in Figure 1. The primary difference in these cells being separate Read, Write, buses required by the 1103. These devices, the most dense of their generation, packaged 1024 bits of RAM in approximately 20K sq. mils of silicon. The 1K device promised ease of implementation when compared to core, and flexible

INTEL 1103 AND MOSTEK 4006
Figure 1



modularity as well as long term cost savings. However, due to unforeseen design complications these devices initially did not achieve thier goal. The 1K RAM started the displacement of core. The next generations, the 4K and 16K dynamic RAMs, all but completed the task.

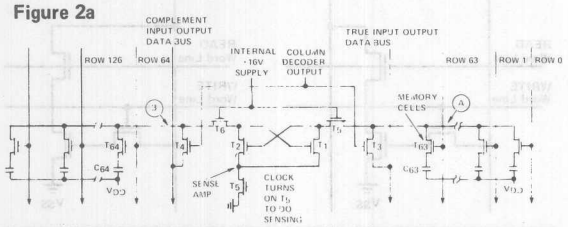
The 4K device, which became the next generation of semi-conductor memory, introduced to the world a wide variance in circuit types available. There were at least 5 major designs available to confuse the user. These were two differently pinned 22-pin devices, two differently pinned 18-pin devices, and a "maverick" 16-pin device which many people thought would never make it. As we all know today, the multiplexed device survived and in fact went on to become the industry standard. This standard pin configuration is presently being utilized in the 16K device as well as its successor the 64K RAM. The first 4K devices utilized a 3 transistor cell similar to that of the early 1K devices. However, N-channel MOS was the technology of all 4K devices rather than P-channel. The inherent advantages of N-channel such as low thresholds for TTL compatibility, faster inherent speed, and greater density, created the incentive needed to develop the required process capability.

The early 3T 4K devices did not survive and were rapidly replaced with the second generation 4K, which utilized a single transistor and capacitor for storage to greatly enhance density. The major problem to overcome with this cell was the small amount of signal available for detection. Several sensing

schemes were developed to handle this problem. One technique utilized a single ended sense amplifier. The balance technique had far better characteristics and became the dominant technique which is utilized today. These different sense configurations are shown in figure 2. It must be appreciated that without development of these sense amplifiers the single transistor cell would not be possible. MOSTEK combined an innovative layout scheme with the balanced sense amp to permit use of active rather than passive load circuits for writing through the sense amplifier. This has resulted in a halving of the dynamic RAM's power dissipation. The 4K devices were well accepted by the user community and slowly but surely began a long but continuous displacement of core memories.

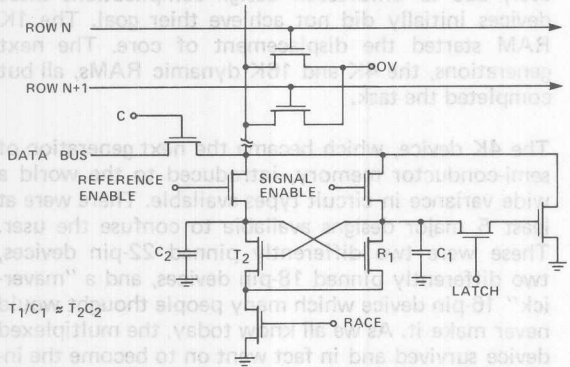
BALANCED SENSE AMPLIFIER

Figure 2a



SINGLE ENDED SENSE AMPLIFIER

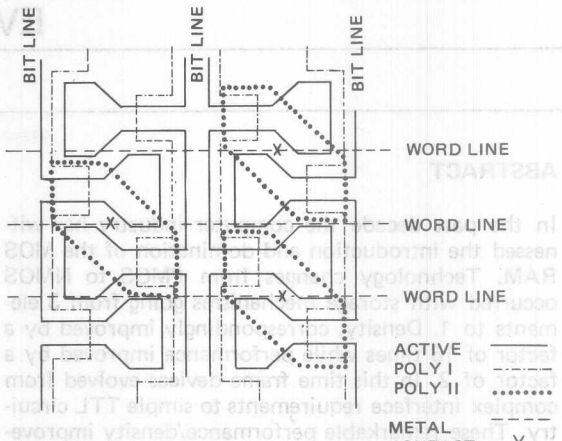
Figure 2b



The MK 4096 introduced by MOSTEK in 1973 established the industry standard pin out. The successor to the 4096 was the revolutionary MK 4027 from MOSTEK which dramatically reduced the die size while dramatically improving the speed. The 4027 set new standards within the industry and established the specification standards that have to be met. The 4027 utilizes MOSTEK's process known as Poly I. This process utilizes a single transistor cell which has an area of about 1.008 mil². The successor to the 4027 is MOSTEK's MK 4116, 16K dynamic RAM. The 16K was made possible by the Poly II™ process which reduced the single transistor cell size to .55 mil². The Poly II™ process utilizes two levels of Poly in the cell location. The implementation of this cell is shown in figure 3.

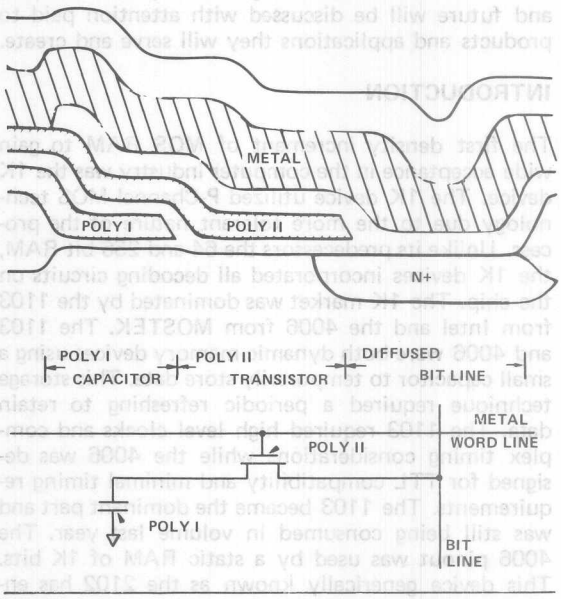
MK4116 CELL LAYOUT

Figure 3a



MK4116 CELL AND CROSS SECTION

Figure 3b

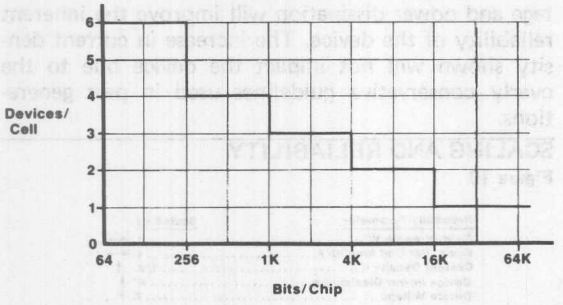


RAM density improvements in the past have come from both circuit and process innovations. The graph of figure 4 shows the evolutionary decrease in the number of devices per cell as a function of density increase. Today we are at a minimum cell configuration, one transistor and one capacitor. The Poly II (TM) process permits packaging the capacitor and transistor in the space of only one device, since no layout space is required to separate these components as in the Poly I process. A further decrease in

the number of components or improvements in layout seems unlikely. Process innovation will, however, continue. In devices through 16K a two dimensional shrinking of dimensions has been employed along with circuit improvement to create a manufacturable die size.

DEVICES/CELL VS BITS/CHIP

Figure 4

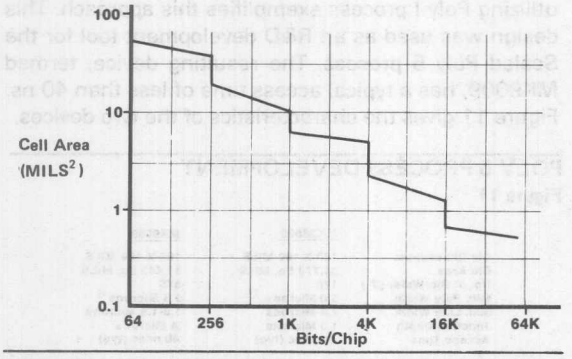


SQUEEZING

In the past device density has increased by reducing the number of elements per cell as well as a two dimensional reduction in geometry. The two dimensional reduction results in a "squeezing" of signal lines and spaces. The graph of figure 5 illustrates the storage cell area advantage gained by this technique.

MEMORY CELL AREA VS BITS/CHIP

Figure 5

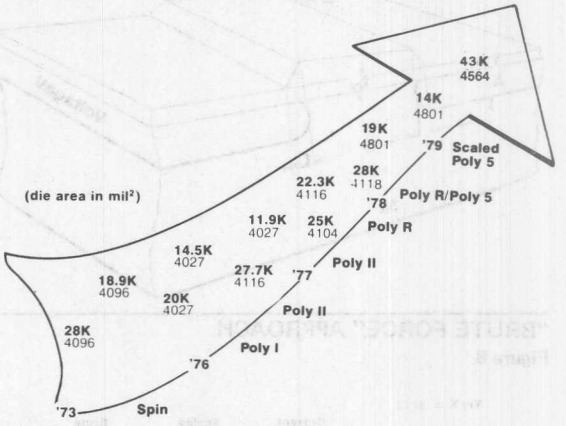


The slope in the graph lines indicate the squeezing mechanism while the verticle steps show cell element reduction. The one anomaly to this lies in the 4K region. Significant area reduction here was achieved by going from the MK 4096 metal gate single transistor cell to the silicon gate single transistor cell of the MK 4027. This required a major technology improvement as did the Poly II (TM) process of the 16K.

Two dimensional squeezing has been used on all previous generation products. Reductions of up to 40% have been realized, for a given design, using this technique. The chart of Figure 6 illustrates the die size and technology evolution of several major products from MOSTEK.

RANDOM ACCESS MEMORY DENSITY EVOLUTION

Figure 6



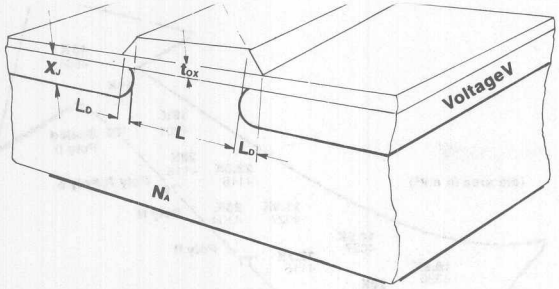
Looking back historically, the replacement of each generation MOS RAM by its successor has taken place by introducing a new memory cell of about one half the area of its predecessor and by tightening design rules used. As a result die size has increased by about a factor of 2 while the number of bits per chip has increased by a factor of 4. It is interesting to note that in evolving from a 64 bit device to a 16K device the RAM circuit density has increased by a factor of more than 50.

The devices per cell now stand at an effective 1, due to the Poly II process. It therefore seems unlikely that a further density improvement will happen here. The next generation will require significant improvement in the remaining area of impact, that is, device geometries. The technique which currently looks the most promising, and is being pursued by multiple companies, is known as scaling.

SCALING

Scaled process technology will be the process which permits the next generation of semiconductor components. "SCALED" refers to circuits in which all physical dimensions, horizontal and vertical have been reduced by scaling factor, as has the operating voltage. This differs from the "squeezing" previously discussed in that 3 dimensions rather than 2 are impacted. Figure 7 shows three dimensional characteristics affected by scaling. In scaling theory all parameters are scaled by a factor K. For a 5 volt part scaled from 12 volts to 5 volts the scaling factor K is 5/12ths. Figure 8 shows MOSTEK's current N-MOS technology compared to resulting geometries based on applying a 5/12ths scaling factor. This approach yields "a brute force" process which will not necessarily be manufacturable. Therefore, a slight modification to the straight-forward scaling technique must be made.

V



"BRUTE FORCE" APPROACH

Figure 8

Try K = 5/12

Device Parameter	Current N-MOS	Scaled By	"Brute Force"
Channel Length L(μ)	5	5/12	2.1
Oxide Thickness t_{ox} (Å)	850	5/12	354
Doping Concentration N_A (substrate resistivity)	10^{15} (10 Ω-cm)	12/5	$2.4x10^{15}$ (6 Ω-cm)
Power Supply Voltage (V)	12	5/12	5
Junction Depth X_j(μ)	1.2	5/12	.45
Lateral Diffusion L_D(μ)	1.0	5/12	.41

The benefits of scaling are numerous. The most significant is that die area goes down by a factor of K^2 permitting the next generation of products. A second benefit of scaling is that device performance increases dramatically thereby permitting the N-MOS technology to participate in a broader applications spectrum than was previously available. The process developed by MOSTEK applying scaling theory is called SCALED POLY 5.

SCALED POLY 5

Scaled Poly 5 is MOSTEK's process for the next generation of products. Scaled Poly 5 is MOSTEK's customized utilization of the scaling theory previously discussed. In the section on Scaling Characteristics, characteristics of "brute force" scaling were shown. Figure 9 gives the key parameters of MOSTEK's process.

SCALED POLY 5

Figure 9

Try K = 5/12

Device Parameter	Current N-MOS	Scaled By
Channel Length L(μ)	5	2.5
Oxide Thickness t_{ox} (Å)	850	500
Doping Concentration N_A (substrate resistivity)	10^{15} (10 Ω-cm)	$5x10^{14}$ (30 Ω-cm)
Power Supply Voltage (V)	12	5
Junction Depth X_j(μ)	1.2	0.4
Lateral Diffusion L_D(μ)	1.0	0.3

The modifications to "brute force" scaling were made to enhance manufacturability, performance and reliability. For example, the low substrate resistivity (6 ohm per centimeter) would result in higher junction capacity and body effect. Both are undesirable traits impacting performance. One must also consider manufacturing tolerance on parameters. This is a definite semiconductor memory days that an unreliable part cannot be applied to products. The scaled Poly 5 process has been optimized to meet MOSTEK's high standards of reliability. Scaling's impact on reliability influencers is shown in figure 10. The decrease in voltage and power dissipation will improve the inherent reliability of the device. The increase in current density shown will not impact the device due to the overly conservative guidelines used in past generations.

SCALING AND RELIABILITY

Figure 10

Reliability Parameter	Scaled by
Field Strength V/t_{ox}	1 ↔
Power Per Unit Area VI/A	1 ↔
Current Density I/A	1/K ↑
Device Power Dissipation	K^2 ↓
Device Voltage	K ↓

1978 was a transition year between process technologies. At MOSTEK, all new products were designed to work on either the 5 micron process or new generation SCALED POLY 5. To accomplish this goal all new products were designed to operate on a single 5 volt power supply. All products use advanced state-of-the-art design techniques and perform very respectably on the standard process. The MK36000 64K ROM which has a typical acess time of 80 ns when manufactured utilizing Poly I process exemplifies this approach. This design was used as an R&D development tool for the Scaled Poly 5 process. The resulting device, termed MK9009, has a typical access time of less than 40 ns. Figure 11 gives the characteristics of the two devices.

POLY 5 PROCESS DEVELOPMENT

Figure 11

	MK36000	MK9009
Die Dimensions	183 X 190 MILS	105 X 109 MILS
Die Area	34,770 Sq. MILS	11,445 Sq. MILS
No. of Die/Wafer (3")	170	575
Min. Poly Width	5.0 Microns	2.5 Microns
Min. Line Width	2.5 Microns	1.0-1.5 Microns
Junction Depth	1.3 Microns	.4 Microns
Access Time	80 nsec (typ)	40 nsec (typ)

SCALED POLY 5 PHOTOLITHOGRAPHIC REQUIREMENTS

We previously discussed the evolution of device/die size to achieve the level of integration required. Correspondingly, device geometries have significantly decreased. Geometry requirements as a fuction of device technology are shown in figure 12. During the evolutionary period from 1960 thru now, geometry requirements have increased by more than a factor of 5. Significant developments have also occurred in photolithographic technology to permit evolution from 1K to 16K. In 1980 our goal was to manufacture devices with two micron dimensions. A quick snapshot of typical equipment used in this segment shows

several problems must be overcome. Today's measuring equipment is accurate to a ± 0.18 microns (10% of what is to be measured). Measurement standards are accurate to ± 0.1 microns. The contact printers have a runout of ± 0.75 microns on 4 inch wafers, a huge percentage of the geometries involved for future technology. Advances in this area are obviously required. These are being attacked and overcome. Methods such as E Beam as well as "step and repeat" printing are available today. These techniques have the ability to address and resolve some of the problems facing the manufacturing aspect of the next generation of technology.

GEOMETRY REQUIREMENTS

Figure 12

	1960	1965	1970	1975	1980
Leading Technology	Discrete	Digital	P-Mos	N-MOS	Poly 5
Line Width (Microns)	10.0	7.0 - 9.0	5.0 - 8.0	3.5 - 5.0	2.0 - 2.5
Interconnect Technology	Metal	Metal	Metal	Metal/Poly	Metal/ Double Level Poly

The key to more complex, cost effective LSI is in Geometry Shrink and Device Creativity.

APPLICATIONS SPECTRUM

Circuit design and technology improvements are continuously opening up new markets for semiconductor memories. The semiconductor industry historically has decreased prices by about 28% with each volume doubling of the industries experience. Fortunately, the RAM market has proven itself to be very price elastic, creating new opportunities at each price level, thereby permitting the necessary increases in volume to keep the trend going.

The memory applications spectrum of Figure 13 indicates the broadening spectrum of the component market. At the left most end of the spectrum, technology improvements resulting in low cost are most significant, while at the right most end performance is key. In fact, the cache and 2900 (4 bit slice) market have previously been dominated by bipolar memory due to the inability of the MOS memory to meet the speed performance required. The introduction of scaled technology is currently permitting N-channel silicon gate MOS to enter this market segment.

MOS-MEMORY APPLICATION SPECTRUM

Figure 13

COST ← PERFORMANCE →

	ELECTRONIC GAMES	MICROPROCESSOR APPLICATIONS	MINI COMPUTERS	MAINFRAME COMPUTERS	CACHE MEMORY
PERFORMANCE	1μS–450nS	450–200nS	250–150nS	200-100nS	100-30nS
PRODUCT	RAM ROM EPROM	SRAM ROM EPROM	D RAM --- ---	D RAM CCD ---	D/S RAM --- ---

MOSTEK will soon introduce several new products which utilize state of the art design techniques as well as the scaled Poly 5 process to expand our penetration into the memory application spectrum.

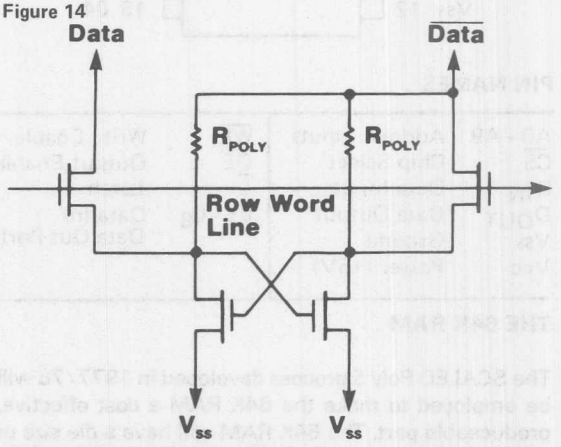
NEW GENERATION PRODUCTS
MK4801

The MK 4801 is a 1Kx8 very high performance static RAM. This device combines a new circuit design technique (address activation) with enhanced process technology to achieve sub 100 nanosecond performance. The circuit will have speed grades available from 55 to 90 nanoseconds. As all new static RAM products from MOSTEK, the 4801 can be manufactured on the Scaled Poly 5 or Poly R process. A typical access/cycle time of 75 nanoseconds at 200 miliwatts dissipation has been measured on devices manufactured on Poly R.

The 4801 uses a unique storage cell design to achieve a very small die size. Figure 14 illustrates this cell. The cell, a mere 2 mil^2, yields a die size of 27,900 square mils when utilizing 5 micron design rules, ala MK 4104. The design technology used yields approximately a 2 times density improvement on the standard process when compared to current generation 4K devices. Application of the Scaled Poly 5 process reduces this die size to approximately 14,000 square mils as well as significantly enhancing performance. Results similar to the 9009 R&D project are anticipated. The 4801 is architectured for speed. The Address Activated ™ interface permits asynchronous operation for the user while maintaining internal advantages of clocked circuit technology. A fast chip select path was designed to permit external decoder delays without impacting access time. The 4801 has been designed for use in all wide word high performance RAM applications.

HIGH PERFORMANCE 4801
2 MIL^2 STATIC RAM CELL

Figure 14

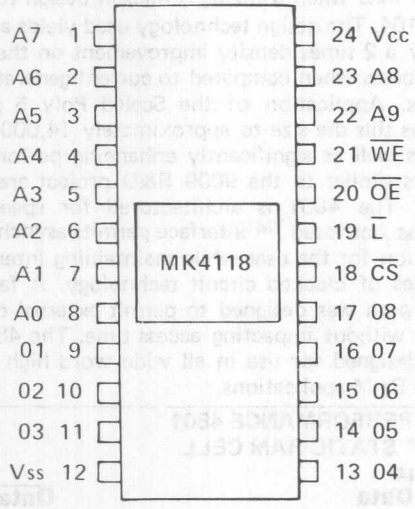


V

MK 4118

The MK 4118 is a sister part to the MK 4801. The part is intended for medium to low speed applications. This device was architectured with next generation as well as existing microprocessors in mind. Speed grades of 120 to 250 nanoseconds will be available. An output enable (OE) and latch (L) function has been included to permit use with common address and data I/O, 16 bit microprocessors. The MK 4118 is packaged in the industry standard 24-pin ROM/PROM compatible configuration shown in figure 15. The device is socket compatible with the 4801 and gives the user a static RAM configuration covering applications from 55ns through whatever. The MK 4118 can be used in an asynchronous mode, like the 4801, or a synchronous mode similar to the MK 4104. The part employs a function called Latch to accomplish the synchronous mode. When activated, LATCH will latch the status of the address and chip select pins. This easy to use memory packages 8K of RAM in an area comparable to a 4K device.

MK4118 PIN OUT
Figure 15



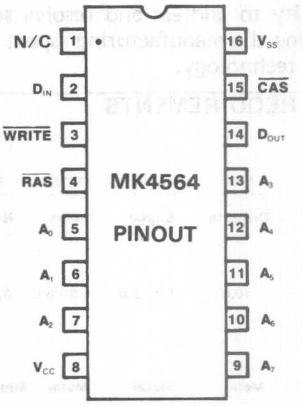
PIN NAMES

A0 - A9	Address Inputs	$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select	$\overline{OE}$	Output Enable
D_{IN}	Data Input	$\overline{L}$	Latch
D_{OUT}	Data Output	$0_1 - 0_8$	Data In/ Data Out Port
Vss	Ground		
Vcc	Power (+5V)		

THE 64K RAM

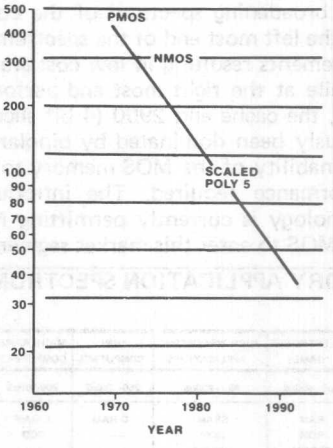
The SCALED Poly 5 process developed in 1977/78 will be employed to make the 64K RAM a cost effective, produceable part. The 64K RAM will have a die size of approximately 40,000 sq mils permitting use of the industry standard 16-pin package. The pin out and key features are shown in Figure 16. Pin 1 is not needed in implementing the basic 64K RAM functionality and will be used as the next address bit for the 256K device.

MK4564 PIN OUT
64K RAM
Figure 16



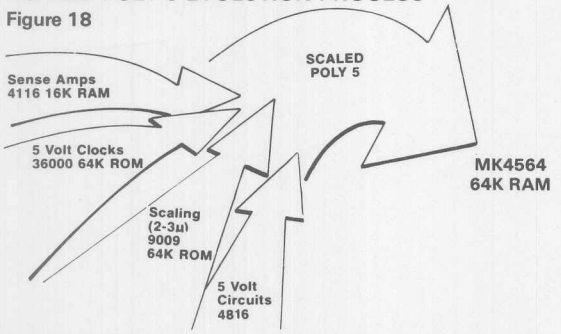
The design goal of the 64K RAM is to have 128 cycle refresh every 2ms making it compatible with its predecessor the 16K dynamic RAM. 128 refresh cycles require use of only 7 of the 8 address pins. To maintain refresh compatibility with previous generation dynamic RAMs, pin 9 (A7) is not used as a refresh address. The 64K being a scaled Poly 5 device uses 2 micron geometries. The device's dissipation is a low 300mw at the operating frequency of the 16K. The MK4564 performance evolution will follow the graph of fig 17.

PROJECT ACCESS TIME FOR DYNAMIC RAMS
Figure 17



The 64K RAM design and process represents a convergence of several developments at MOSTEK during the past several years. The techniques needed to achieve a useable 64K RAM, required several break throughs which are currently being proven on predecessor parts. Figure 18 illustrates the evolutionary process required to develop this major product.

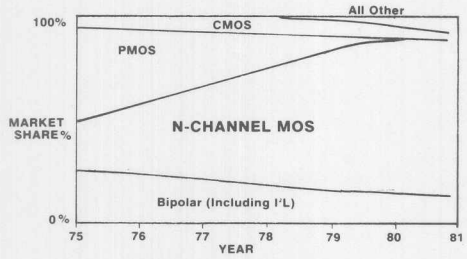
SCALED POLY 5 EVOLUTION PROCESS
Figure 18



CONCLUSION

N-channel Silicon Gate MOS will continue to dominate the memory market. New technology break-throughs such as Scaled Poly 5 and Address Activated design techniques will permit NMOS to conquer new market segments. Smaller die sizes and increasing volumes will continue to reduce costs, thereby further expanding the market. The chart of figure 19 illustrates the memory market share by technology. In conclusion, N channel MOS will continue to expand its application spectrum and remain the dominant technology in the 80's.

MEMORY MARKET SHARE BY TECHNOLOGY
Figure 19



GLOSSARY OF PROCESS NAMES

SPIN - Metal gate N channel process. (Self-aligned Poly Interconnect N-channel)
POLY I - Single level Poly N-channel Silicon gate
POLY II - Double level Poly N-channel Silicon gate
POLY R - Single level Poly N-channel Silicon gate incorporating Poly Silicon Resistive loads.
SCALED POLY 5 - Double level Poly N-channel Silicon gate ion implant.

V

1982/1983 MEMORY DESIGNERS GUIDE

1982/1983 MEMORY DESIGNERS GUIDE

MOSTEK CHIP CARRIERS

Since 1978 Mostek has been supplying the MK4116E leadless chip carrier (LCC) to the data processing industry. The millions of devices shipped to date allows Mostek to produce and test the LCC as a mainstream device with the cost benefits helping both the manufacturer and the user. This ongoing commerical volume contrasts the next emerging market for the LCC which is the military. An extensive development effort aimed at both the user community and the IC manufacturers has resulted in a much broader availability, but with lower volumes. Mostek is able to address both of these markets and share the benefits of volume with both.

While the availability of the loose LCC is important, many users are concerned with their ability to use surface mount devices in their existing production environment. They have found that when LCCs are mounted on a leaded ceramic substrate, they can be handled in the system environment just like a DIP. Mostek meets this need with the RAM-PAK™. The standard RAM-PAK configurations are listed below. This concept applies to all LCCs and where a common configuration is needed by a wide customer base, Mostek can turn it into a standard product.

COMMERCIAL PRODUCTS IN CHIP CARRIERS

Device	LCC	Size	Description	Speeds
MK4104E	18 Pad	.285 x .350	4K x 1 SRAM	–4, –5
MK4116E	18 Pad	.285 x .350	16K x 1 DRAM	–2, –3, –4
*MK4167E	20 Pad	.285 x .425	16K x 1 SRAM	–1
MK4516E	18 Pad	.285 x .350	16K x 1 DRAM	–2, –3
MK4564E	18 Pad	.285 x .425	64K x 1 DRAM	–2, –3
MK4332D	18 Pin	RAM-PAK	32K x 1 DRAM	–3, –4
*MK4528D	18 Pin	RAM-PAK	128K x 1 DRAM	–3, –4

MILITARY PRODUCTS IN CHIP CARRIERS

Device	LCC	Size	Description	Speeds
MKB2716E	32 Pad	.450 x .550	2K x 8 EPROM	–88
*MKB37000E	32 Pad	.450 x .550	8K x 8 ROM	–84
MKB4104E	18 Pad	.285 x .350	4K x 1 SRAM	–85, –86
MKB4116E	18 Pad	.285 x .350	16K x 1 DRAM	–83, –84
*MKB4167E	20 Pad	.285 x .425	16K x 1 SRAM	–81
MKB4516E	18 Pad	.285 x .350	16K x 1 DRAM	–82, –83
*MKB4564E	18 Pad	.285 x .425	64K x 1 DRAM	–83, –84
MKB4802E	32 Pad	.450 x .550	2K x 8 SRAM	–81, –82
MKB4332D	18 Pin	RAM-PAK	32K x 1 DRAM	–83, –84
*MKB4528D	18 Pin	RAM-PAK	128K x 1 DRAM	–83, –84

*To be introduced in 1982

SYSTEM CONSIDERATIONS FOR USING MEMORIES IN LEADLESS CHIP CARRIERS

Application Note

The leadless chip carrier is an integrated circuit package which has been developed to address certain limitations in the dual in-line package. Since a major thrust was begun in 1976 investigating the characteristics of the LCC (also called the HCC or hermetic chip carrier), a number of articles have appeared discussing the basic package. Referred to as "one of the smoothest, most well-thoughtout and comprehensive standardization programs the electronics industry has ever produced"[1], the Joint Electron Device Engineering Council (JEDEC) has layed out package standards in advance of mass production. As the balance of the IC makers join the initial thrust, the user community is seeing a common thrust where divergent approaches normally exist.

Besides multiple sources of supply, cost and availability are a concern to potential users. All three of these factors are dependent upon volume production and the mainstream effects it produces. The key here is that the first high volume LCC will be the one experiencing the highest usage. In most processing applications these are the memories. Memories have this distinction for most data processing applications.

REASONS FOR LCC USAGE

The original justifications for developing the LCC as an integrated circuit package addressed many of the same shortcomings of the DIP as the flat pack attempted to. The DIP is large and heavy and as the pin count increases these problems are aggravated. Table 1 details the size and weight issue, but more important for some applications are the electrical characteristics.

The resistance and inductance from the corner pins to the die become significant for high speed functions; particularly for the larger DIPs. Advancing technology and the VHSIC program will result in higher speed functions, so the LCC's 4 GHz speed will prove superior to the DIP's 500 MHz limit for these applications.[1]

Engineering justifications for examining LCCs have been well addressed in the literature and the reader is invited to refer to the bibliography to gain insight into research done to date. This research confirms that the LCC is a viable packaging option for the near future. Packaging density and economics have surpassed the more esoteric reasons for using LCCs and have made the near future the recent past. As this paper will discuss, the gains available with LCCs can be obtained by anyone using memory products in DIPs.

MEMORIES IN LCCs

When analyzing the contribution each part type makes when building a system, memories are often the largest hog of PWB real estate. In memory intensive computers and information handling systems, multiple boards can be filled with arrays of a single part type, generally the MK4116 16K x 1 dynamic RAM. The density lesson was well learned by Mostek many years ago when the entire industry was surprised at the success of the 4K x 1 MK4096. Prior to its introduction, a 22 pin DIP 400 mils wide was the industry standard. By multiplexing the row and column addresses, Mostek was able to offer the same number of bits in a 16 pin DIP 300 mils wide. The complete acceptance of this concept which did add complexity in the peripheral circuitry is evident in that all 16K, 64K, and 256K designs are still appearing in that same 16 pin DIP.

Chip carriers present an opportunity for military and commercial manufacturers to half again their PWB real

VI

MECHANICAL CONSIDERATIONS

Table 1

# OF LEADS		PACKAGE AREA sq. in.		PACKAGE WEIGHT grams	
DIP	LCC	DIP	LCC	DIP	LCC
16	18	0.24	0.10	1.4	0.4
16	20	0.24	0.12	1.4	0.5
24	32	0.72	0.25	4.7	0.9
40	44	1.20	0.42	6.4	1.6
64	68	2.88	0.90	12.11	3.2

1) 50 mil lead spacing leadless type B packages
2) 18 pad and 32 pad are rectangular LCCs

estate committed to memory. Mostek and a major EDP manufacturer developed an approach to the problem of density which resulted in the introduction of the 32K x 1 MK4332D Dynamic RAM in 1978 (Figure 1). By placing two MK4116's in chip carriers side-by-side on a DIP daughterboard, an end user could reap the advantages of LCCs while retaining his manufacturing techniques which are set up for a DIP world. The results of this are significant in that through mid 1981 over 3 million MK4332's have been shipped. The mainstream effect which is desired and can be obtained with the help of commercial usage has happened, with the effects on cost, delivery and volume availability all quite positive. So the lose LCC is for real, but the question the MK4332 addressed and the question most people ask first is: How do you use them?

REFLOW SOLDERING

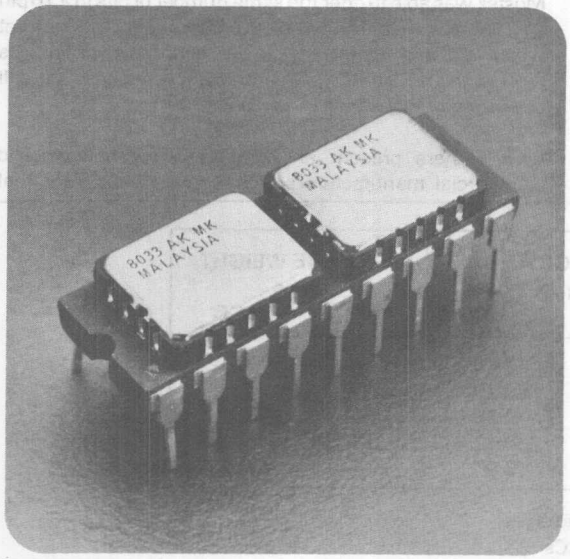
Direct attachment to a substrate is performed with a reflow soldering operation. Differing methods exist for this operation since many manufacturers have experience in reflow soldering flat packs, chip capacitors and other surface mount devices. Basically, either one or both of the surfaces is pretinned with solder prior to the component being placed onto the joint. The temperature of the joint is then raised to the melting point of the solder, where the solid solder turns molten, wetting to itself and forming a single, quality solder joint.

With a LCC array, the above process becomes much more involved than the familiar process of "tacking" a capacitor onto a PWB with reflow soldering which we are all familiar with. The following discussion will list various options in design, materials and processes which have been successfully used. As with any proposed manufacturing method, an element of fine tuning will need to occur in each individual setup to obtain optimal results.

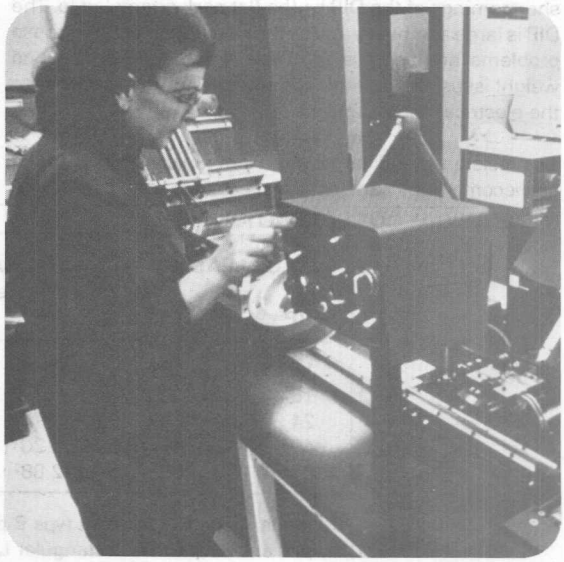
A pattern of footprints will be seen on the surface of the PWB or the ceramic substrate. Solder paste is applied to these footprints with normal silkscreening methods. The variables introduced at this point are the thickness of the silkscreen (determining the height of the solder buildup) and the solder paste characteristics. The solder paste includes grains of solder (Sn63 or Sn60) plus a resin flux. Following the first screening, the board is brought to the reflow temperature of the solder, forming even bumps on each of the equally sized pads. This step may be replaced by a nonfuzed solder plate on the board. This initial step achieves a two fold goal: confirmation of the solderability of the board and an initial buildup of the solder which will contribute to the eventual gap which will develop between the LCC and the PWB.

A repeat of the screening operation will be performed next, except that the tacky nature of the solder paste will not go to waste. Following the solder screening, the LCCs can be placed down lightly onto their footprints where they will be held fast against normal handling shock by the solder paste. Several variables are introduced here in the treatment of the LCC pads and the handling the parts are to receive prior to reflow. Mostek's RAM-PAK™ assembly line exemplifies one extreme of conditions in that a run rate of 50K pieces a week can be maintained on a single part type (Figure 2). The benefits which Mostek enjoys are not shared by the majority of the industry. The LCCs which Mostek uses suffer few of the normal abuses which an IC experiences between the factory and the final time and place where it is soldered. As any manufacturing manager can tell you, solderability will

MK4332 ACHIEVES DOUBLE DENSITY OVER THE DIP
Figure 1



RAM-PAK ASSEMBLY LINE CAN PRODUCE 50K UNITS PER WEEK
Figure 2



decrease with storage time. Therefore, Mostek can get away with placing untreated LCCs onto the solder paste and running them through the furnace.

Another key advantage which can only be gained by volume is the streamlined flow shown in Figure 2. Following pick and place, the RAM-PAKs™ are transferred onto the belt of an IR furnace. As the parts exit the furnace, they fall into a solvent, where they accumulate prior to being subjected to a conventional vapor degreasing operation. RAM-PAK™ parts have other advantages due to their simple configuration. Inspection may be easily performed visually due to the 5 mil gap under the LCCs. The systems user performing his own reflow operation will typically have neither the ability to inspect visually, nor the 5 mil height of the air gap due to reasons discussed soon.

A flow in which an end user finds more satisfaction involves a pretinning of the individual LCCs by floating them in a solder pot. The solder bump on the LCC pad not only allows an inspection of the surface solderability, but also adds to the quantity of solder in the final joint. This pretinned LCC is placed on the same surface as described earlier, except instead of going straight into a furnace, the assembly is dried at about 80°C to drive the solvents from the flux. At this point, a prepared unit awaits the choice of heating methods.

WHAT TYPE OF FURNACE

In a reflow soldering operation, no solder is added to the board during the actual soldering. What is needed is for the board surface to be brought up to the eutectic point of the solder, where the prewetted joints become molten again and a single fillet results where two distinct surfaces once were. Various furnaces have differing advantages but the technique which is most commonly identified with LCCs is Vapor Phase.

Vapor Phase reflow soldering has been brought to a production reality by HTC Corp.[9] Truly a reflow technique, Vapor Phase works by emersing the relatively cool parts into boiling FC-70, an inert fluorocarbon manufactured by the 3M Company. As the FC-70 vapor condenses on the assembly, it is quickly and uniformly heated to the boiling temperature of the fluid. Since FC-70 has a boiling point of 215°C, any properly prepared joints quickly reflow. The reasons that Vapor Phase soldering has become synonymous with LCCs have to do with the uniformity of heat application and the repeatability of results over a variety of part types. But Vapor Phase does suffer from the high cost of FC-70 fluid, and for well controlled volume-runs other heating methods deserve consideration.

Mostek's RAM-PAK™ assembly line uses an IR furnace to attach LCCs onto cofired ceramic substrates. This method is not without fault in that the gold lids reflect the IR energy. For a high volume assembly which can be characterized over time, proper belt speed and energy levels can be determined to achieve an acceptable quality level; however, the amount of learning required with this method could cause excessive reject rates on small volume runs. Convection furnaces and controlled temperature hot plates may be used with success. Since LCC attachment is simply a heating process to reach reflow temperature, any heating method can work.

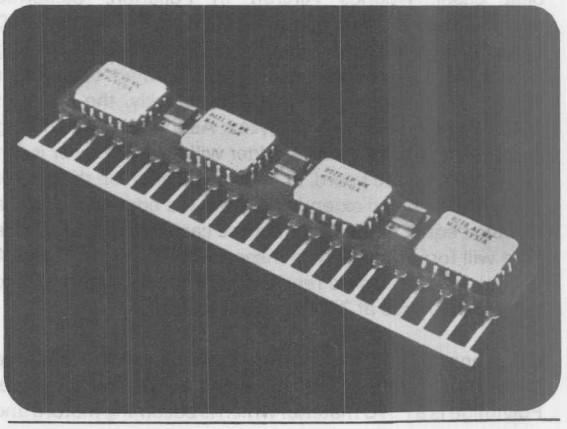
CHOOSE YOUR SUBSTRATE

The preceeding soldering techniques can be used on any type substrate, so the material is typically chosen on the basis of system constraints and not processing limitations. The factors which should be considered beyond the thermal characteristics are touched upon here.

How a system is partitioned affects the system in many ways. Enclosure costs, manufacturing costs and repairability are all affected. Due to the limited size of a single piece of ceramic, placing LCCs onto a ceramic substrate which in turn has leads is an easy way for a house to begin utilizing LCCs. The MK4332 RAM-PAK™ shown earlier represents a minimal configuration with two MK4116E's mounted on a ceramic daughterboard. Many houses can now successfully use LCCs by buying the assembled MK4332D. The ceramic motherboard concept can be further expanded to the 16K x 4 memory in a single in-line package for vertical mounting, or into 4, 8 or more chips per substrate as the designer chooses. A variety of substrates are available which are designed to accept the MK4116E including the substrate shown in Figure 3.

The ceramic substrates discussed so far reflect a near unanimous verdict in terms of deciding upon the material to be used in LCC systems. Since direct attachment via reflow soldering is the preferred method of LCC attachment,

DENSITY CAN BE QUADRUPLED USING THIS SIP SUBSTRATE AND MK4116Es
Figure 3



require as it is cycled over temperature (generally implying a transition of -55°C to +125°C). When materials of differing TCEs are bonded together, the bond must either flex or be strong enough to withstand the resulting forces. Table 2 gives the TCEs for LCCs and for a number of popular (or potential) substrates. As the table shows, ceramic on ceramic will result in the lowest mismatch and therefore, the highest joint reliability.

Ceramic is not as difficult to use as may seem. The DIP and SIP concepts previously discussed can easily be modified to handle other configurations, and the smaller user doesn't need to handle the assembly right away. Many hybrid houses accept this business and can provide design and assembly services to the user community. New designs will typically prototype with thick film ceramics which employ multiple screening layers upon a single preformed piece of ceramic. As volumes approach the one thousand piece level, conversion to cofired ceramic becomes cost effective. Here each screening layer is put on a separate sheet of greenware which is then stacked and fired. The resulting ceramic assembly is effectively a solid piece of ceramic with all electrical connections internal. Cofired ceramics have been assembled up to 43 layers this way and in fact it is the assembly method for the 3 layer style LCC package which is being offered by most IC manufacturers.

While ceramic does have a number of virtues which are prompting its use, it is heavy, it breaks and there is a maximum size constraint. Combine these factors with the observation that ceramic LCC assemblies are generally daughterboards which then go into a PWB motherboard and the question arises, "What about direct attachment to PWBs?".

The number one problem with this is joint reliability. The obvious worst case example is large (over 40 pad) LCCs mounted onto G-10. This combination has repeatedly been tested with consistently poor results. But what about the best case? Hughes Aircraft in Fullerton, California examined the problem of attaching 18 pad LCCs onto G-10 glass epoxy PWBs and came up with some interesting results. Since previous work demonstrated that solder joints directly under LCC pads fail quickly, the effect of extending the pads was analyzed. As the reflow soldering process occurs, the molten solder will flow wherever it can along the pad, the board, and the castillation on the side of the LCC. If the pad extends out from the edge of the LCC a distance equal to the height of the castillation, then a nice fillet will form. The easy to inspect fillet shown in Figure 4 also provides a degree resiliency which allows the joint to survive in excess of 200 thermal cycles.

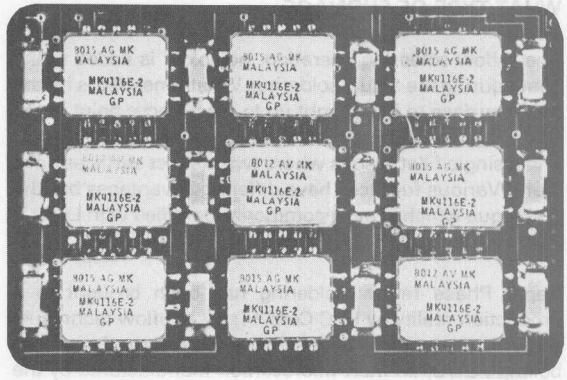
Glass epoxy G-10 has the worst TCE shown in Table 2 so the other materials offer even better performance. Polyimide is a PWB material which is becoming mature and even better TCEs result. However, cutting and drilling become problems. This can be understood since Kevlar's other uses include tire cord and bullet proof vests.

Metal core and laminate type circuit cards offer other ways of getting better TCEs. Stitched wire type interconnects on Kovar are becomming available. Other approaches using porcelain coated steel and copper laminates are also being studied.

The entire subject of LCC attachment, reliability and repairability is being studied under Air Force contracts. These studies will complement the work going on in many military manufacturers and will greatly increase our understanding of mounting LCCs during the next year.

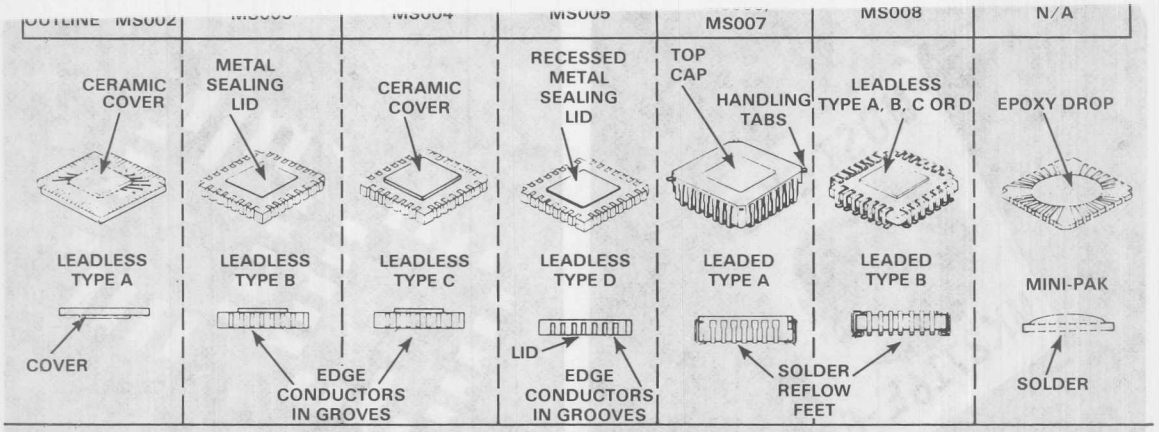
GOOD FILLITS BENEFIT JOINT RELIABILITY WHEN ATTACHING DIRECTLY TO ORGANIC PCBs

Figure 4



REPLACEMENT OF BAD LCCs

So far manufacturing techniques have been described which are applicable at the assembly level, but what about repair of LCC assemblies? When a ceramic substrate is used, it can simply be placed back onto a hotplate where the defective LCC is lifted off with a vacuum pencil once the solder melts. A pretinned replacement unit is simply dropped into place where the surface tension of the molten solder will align it. Repairing PC boards containing chip carriers is more difficult, but then so is removing defective DIPs. One method in use involves a specially made "soldering tong" which clamps onto all 4 sides of the LCC, heating up the device. Again, replacement should be the



opposite of removal when a pretinned LCC is used. These tongs are low cost and readily available.

POWER DISSIPATION

Integrated circuit reliability has an established relationship to junction temperature, so an effective thermal design is a must in today's hi-rel conscious environment. LCCs offer the system designer some unique opportunities for creative design due to their surface mount nature. The JEDEC standards have recognized this in the formation of two basic types of carriers. The type A and type D carriers are "cavity down". As Figure 5 shows, the die is closer to the top and the best heat radiating surface is the top. But an extra penalty is paid in that the package outside dimension will have to be larger for a given die size. The types B and C carriers will be more common for that very reason, recognizing the importance of density.

So most LCCs will have a "cavity down" configuration with the major heat radiating surface facing the board. Tests show that the thermal resistance of the LCC itself is roughly equivalent to that of a ceramic DIP, so the mounting method will directly impact the junction temperature. Two types of heat transfer occur; conduction and convection. Most commercial systems employ forced air and convection cooling, so surface area is a key to good heat transfer. The daughterboard approach such as used with the SIP is a perfect blend of PWBs and LCCs in that they can be mounted vertically, or "corn rowed"[3]. Not only is the density greater than with surface mounted LCCs, but forced air can be used to keep the assembly cool.

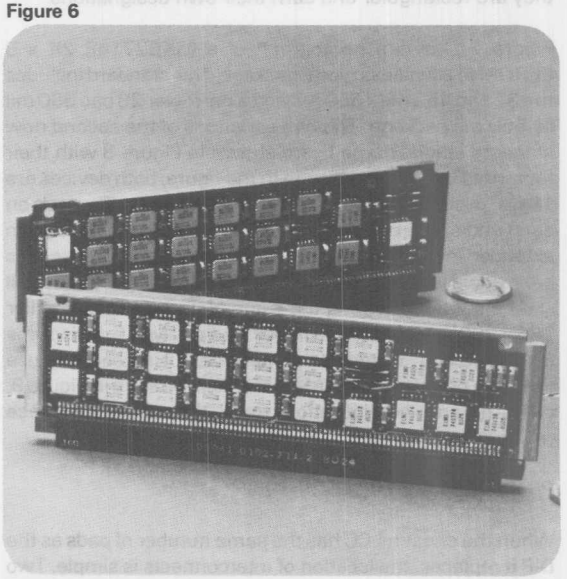
Most military manufacturers and some commercial ones do not have the luxury of sucking in outside air through a fan and blowing it around their devices. They rely on conduction to transfer the heat through the frame to an outside heat sink. They are concerned about the thermal properties of their substrates since the heat will go through the pads and out.

The thermal conductivity data in Table 2 shows that solid metals are great for removing heat, but poor in TCE match. So a solution such as the SEM in Figure 6 can be used. Here a multilayer G-10 PWB is bonded to a copper frame, with an identical PWB on the other side for a 32K x 16 memory module. The bonding compound would need to be compliant since the copper is for rigidity and thermal transfer and is not meant to force a TCE match. Other metal core approaches do use metal for TCE match and pick up the thermal conductivity as an added benefit.

PACKAGING STANDARDIZATION

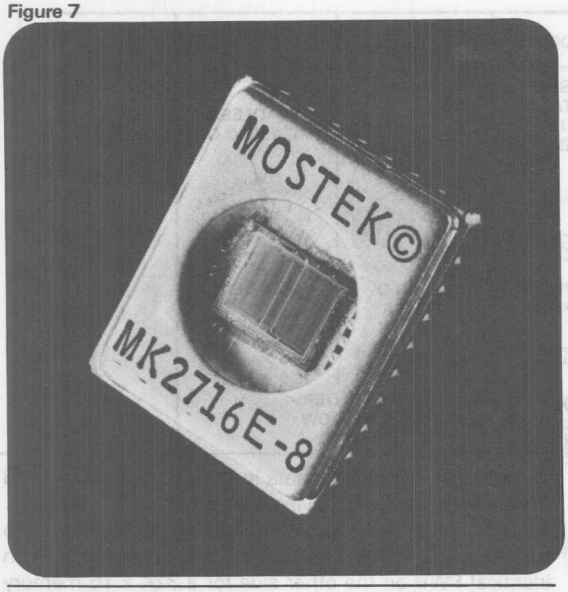
The mechanical configuration for a family of LCC packages has been defined for years now.[4] Types A, B, C, and D

MILITARY USER OBTAINS 32K x 16 DENSITY ON A NAVY SEM MODULE (Photo courtesy Hughes)
Figure 6



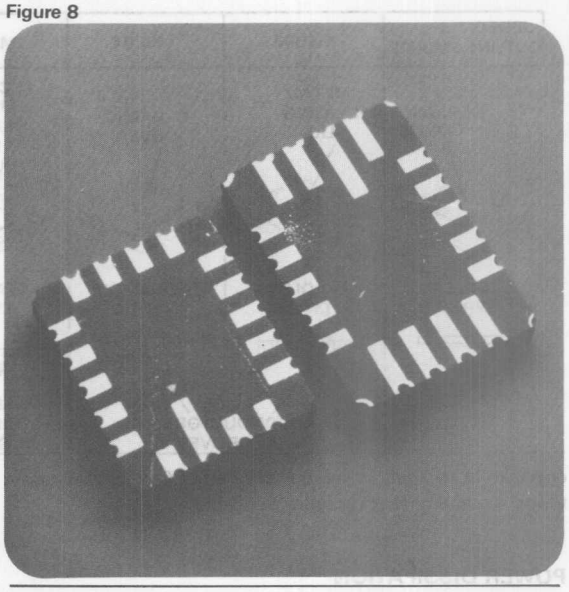
MK2716E HAS 2K x 8 OF UV ERASABLE EPROM IN A 32 PAD LCC

Figure 7



COMPATIBILITY CAN BE KEPT AS THE 16K RAM IS 'STRETCHED' TO THE 64K

Figure 8



packages for a range of sizes have been defined and made available. These standard square packages have made it possible to purchase many logic functions in LCCs from both the logic manufacturer or their die distributors.

Memory ICs naturally differ from the earlier SSI and MSI ICs. Their die tend not only to be much larger, but they also tend to be rectangular instead of square. Combining these reasons with the natural advantage of memories to be in rectangular packages to aid in PC board mounting, and two new JEDEC package types result. While both of these new types are similar to the square type C LCC in construction, they are rectangular and earn their own designations.

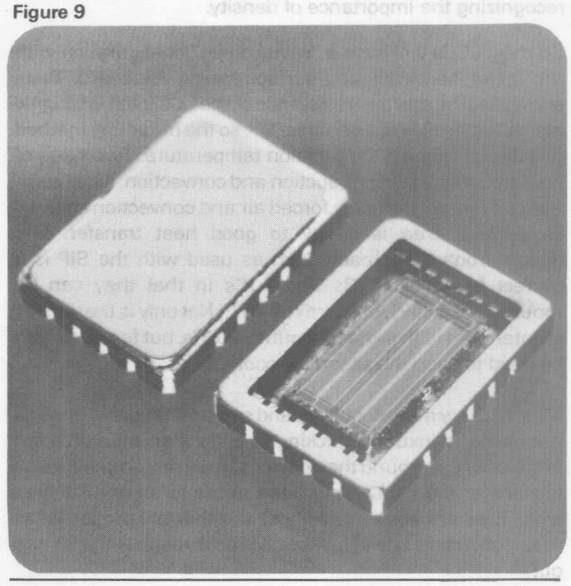
Figure 7 shows a photograph of a MKB2716E 2K x 8 EPROM in a leadless type E package. This standard includes the 32 pad 450 mil x 550 mil and a narrower 28 pad 350 mil by 550 mil package. The two variations of the second now standard leadless type F, are shown in Figure 8 with their footprints up. As can be seen in the figure, both devices are 18 pad packages with an interesting difference. The pads on each end of the longer 425 mil x 285 mil device have been extended inward. In this way, compatibility on the board has been achieved because the footprint of the larger device will extend inward, covering the same footprint as the smaller 285 x 350 mil device. The larger leadless type F device was not "stretched" to add additional pads, but instead to house the large 64K dynamic RAM die. As can be seen in Figure 9, die size and configuration force the usage of these rectangular LCCs to obtain optimal packing density.

PINOUT STANDARDIZATION

When the chosen LCC has the same number of pads as the DIP it replaces, the location of interconnects is simple. Two examples are 4K x 1 and 16K x 1 static RAMs. However, when extra pads appear, an opportunity arises for differences to develop between vendors. Fortunately, a defacto standard has resulted for dynamic RAMs based upon Mostek's MK4116E chip carrier which has been offered since 1978. Most dynamic RAM suppliers are planning on offering their 16K and 64K parts with the pinout shown in Figure 10. In addition, the 20 pin MK4167 will be available in a 20 pad chip carrier which is 425 mil x 285 mil.

64K DYNAMIC RAM TAKES FULL ADVANTAGE OF THE SPACE IN THE LCC

Figure 9



Bytewyde™ memories in 32 pad type E 450 mil x 550 mil LCCs have not enjoyed similar "upfront" standardization efforts. Two pinouts currently exist for the 2716 (Figure 7), each based upon the requirements for the next generation 64K EPROM. The pinout shown in Figure 11 takes advantage of the 32 pads to produce a configuration accepting all current and future members of the JEDEC family of by 8 RAMs, ROMs and EPROMs.

LCCs AND THE MILITARY

Major new usage of LCCs is being promoted by many military manufacturers. The impact of this is that device availability will start with parts screened to MIL-STD-883 Class B, followed sometime later by "commercial grade" devices. Attachment research is centered with military contractors as well. Besides the Air Force sponsored work mentioned earlier, independent research on production techniques is addressing the finer points of LCC usage such as repairability, vibration and thermal conduction improvements. The user should look to the military community and their manufacturing publications for an up-to-date status of this research.

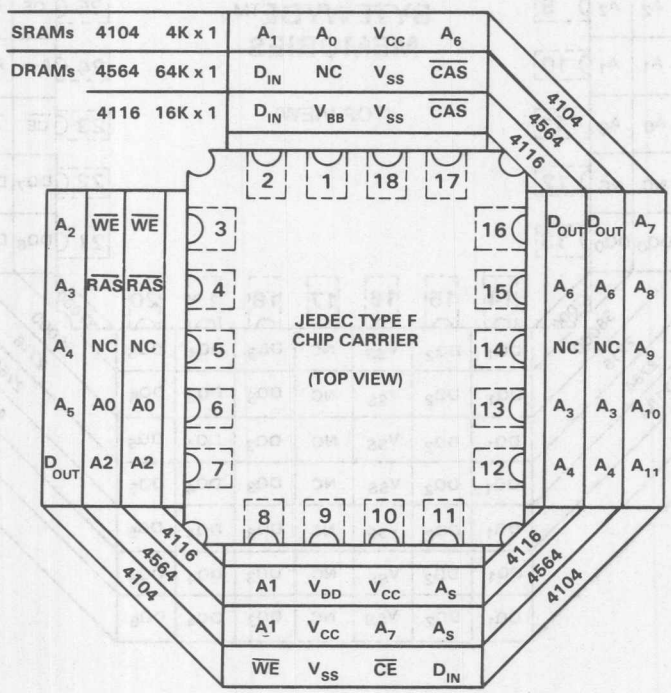
LCCs AND THE FUTURE

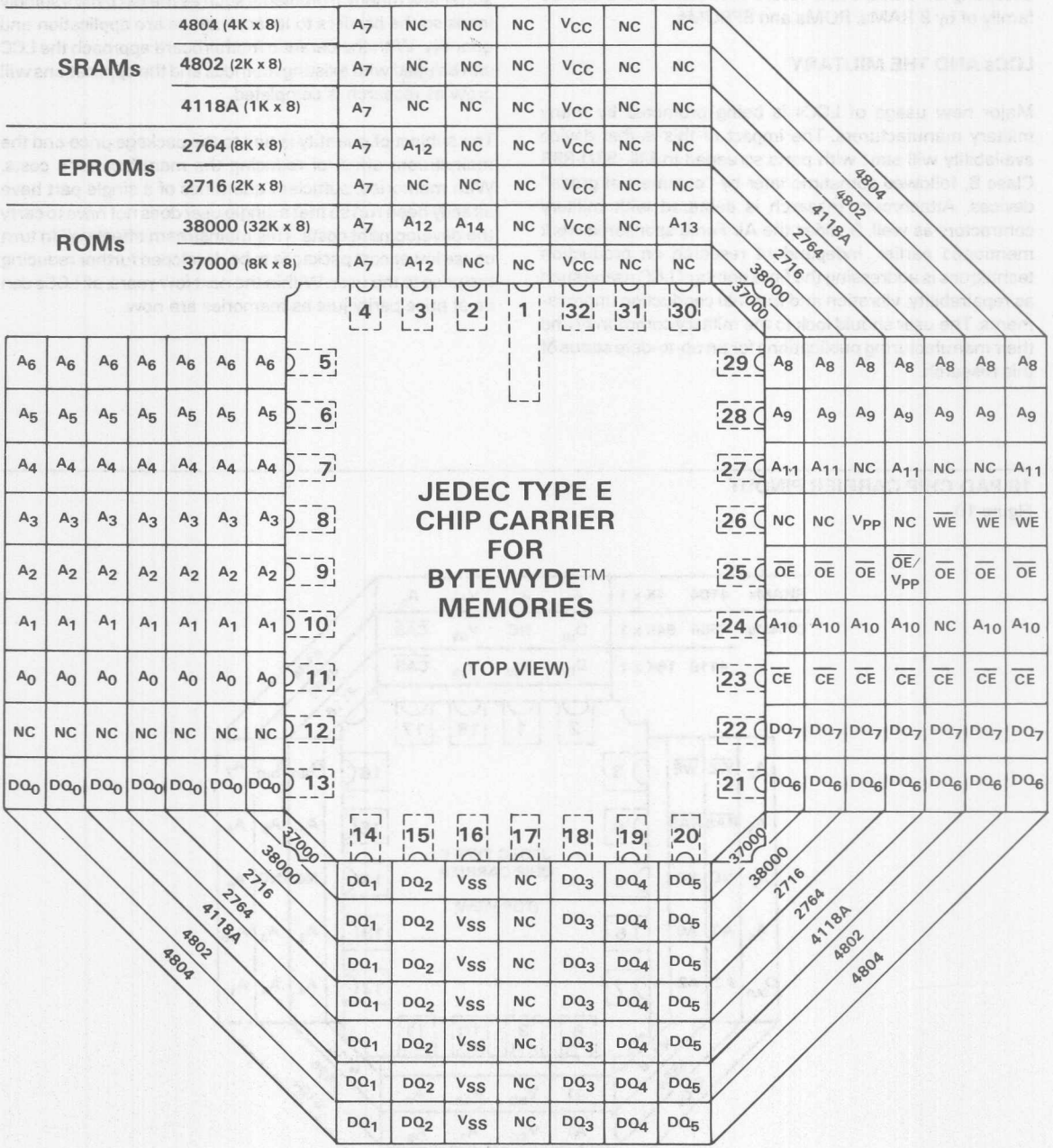
Whether the leadless chip carrier grows into a competitive volume package, or remains a premium specialty part depends upon how well it is embraced by all segments of users. At this time the three layer ceramic LCC appears to suffer few inherent problems such as the flat pack's spindly leads so the barriers to its acceptance are application and quantity. With the ceramic motherboard approach the LCC can be used with existing methods and the applications will grow as research is completed.

The subject of quantity is tied to the package price and the mainstream effect of reducing the manufacturer's costs. With memories, sufficient quantities of a single part have already been run so that a single user does not have to carry the development costs. This mainstream effect will in turn cause lower cost packages to be developed further reducing the price to the user. Within the next few years, all LCCs can be at price parity just as memories are now.

18 PAD CHIP CARRIER PINOUT

Figure 10




SRAMs
4804 (4K x 8)
4802 (2K x 8)
4118A (1K x 8)
EPROMs
2764 (8K x 8)
2716 (2K x 8)
ROMs
38000 (32K x 8)
37000 (8K x 8)
JEDEC TYPE E
CHIP CARRIER
FOR
BYTEWYDE™
MEMORIES
(TOP VIEW)
4804
4802
4118A
2764
2716
38000
37000

THERMAL EXPANSION COEFFICIENTS

Table 2

MATERIAL	TCE (ppm/°C)	% DIFFERENCE FROM EXPANSION IN LCC	THERMAL CONDUCTIVITY BTU/HR Ft^2 °F
90 to 94% alumina LCC package	6.5	—	9.6
96 to 99.5% alumina thick film substrate	6.8	5%	12
90 to 94% alumina cofired substrate	6.5	0%	9.6
Epoxy-glass (G-10)	18	177%	.17
Polyimide-glass	13	100%	
Polyimide-Kevlar	5.5	15%	
Alloy 42 .025"	5.8	11%	8.8
Steel .025"	10	54%	27

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90 to 94% alumina LCC package	6.5	—	9.6
88 to 89.3% alumina thick film substrate	6.9	6%	12
90 to 94% alumina sintered substrate	6.5	0%	9.6
Epoxy-glass (G-10)	18	177%	1.7
Polyimide-glass	13	100%	
Polymide Kevlar	6.5	0%	
Alloy 42 .020"	5.3	77%	8.9
Silver .020"	10	54%	27

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